

HD6809, HD68A09, HD68B09

MPU (Micro Processing Unit)

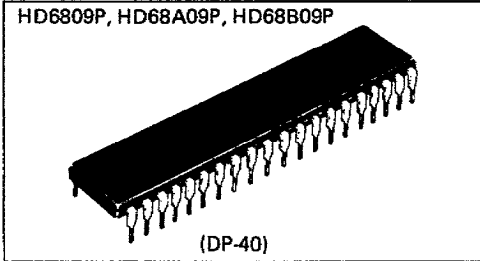
The HD6809 is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the HMCS6800 family has major architectural improvements which include additional registers, instructions and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The HD6809 has the most complete set of addressing modes available on any 8-bit microprocessor today.

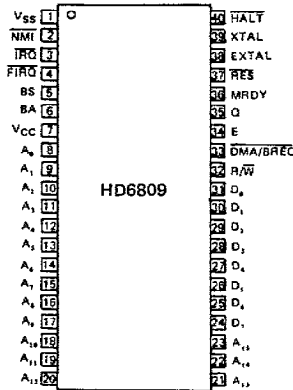
The HD6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

HD6809P, HD68A09P, HD68B09P



(DP-40)

■ PIN ARRANGEMENT



(Top View)

HD6800 COMPATIBLE

- Hardware – Interfaces with All HMCS6800 Peripherals
- Software – Upward Source Code Compatible Instruction Set and Addressing Modes

■ ARCHITECTURAL FEATURES

- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

■ HARDWARE FEATURES

- On Chip Oscillator
- DMA/BREQ Allows DMA Operation or Memory Refresh
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- MRDY Input Extends Data Access Times for Use With Slow Memory
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle RESET
- Single 5-Volt Supply Operation
- NMI Blocked After RESET Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories
- Compatible with MC6809, MC68A09 and MC68B09

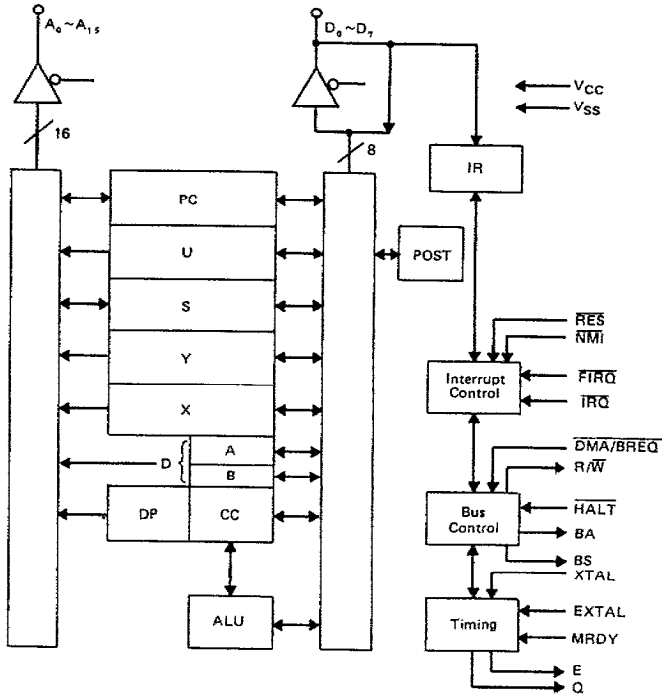
■ SOFTWARE FEATURES

- 10 Addressing Modes
 - HMCS6800 Upward Compatible Addressing Modes
 - Direct Addressing Anywhere in Memory Map
 - Long Relative Branches
 - Program Counter Relative
 - True Indirect Addressing
 - Expanded Indexed Addressing:

0, 5, 8, or 16-bit Constant Offsets
 8, or 16-bit Accumulator Offsets
 Auto-Increment/Decrement by 1 or 2

- Improved Stack Manipulation
- 1464 Instructions with Unique Addressing Modes
- 8 x 8 Unsigned Multiply
- 16-bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V _{CC} *	-0.3 ~ +7.0	V
Input Voltage	V _{in} *	-0.3 ~ +7.0	V
Operating Temperature	T _{opr}	-20 ~ +75	°C
Storage Temperature	T _{stg}	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

(NOTE) Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	
Supply Voltage	V _{CC} *	4.75	5.0	5.25	V	
Input Voltage	V _{IL} *	-0.3	-	0.8	V	
	V _{IH} *	Logic (T _a = 0 ~ +75°C)	2.0	-	V _{CC}	V
		Logic (T _a = -20 ~ 0°C)	2.2	-	V _{CC}	
\overline{RES}	4.0	-	V _{CC}			
Operating Temperature	T _{opr}	-20	25	75	°C	

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, T_a=-20~+75°C, unless otherwise noted.)

Item	Symbol	Test Condition	HD6809			HD68A09			HD68B09			Unit	
			min	typ*	max	min	typ*	max	min	typ*	max		
Input "High" Voltage	Except \overline{RES}	T _a = 0 ~ +75°C	2.0	-	V _{CC}	2.0	-	V _{CC}	2.0	-	V _{CC}	V	
		T _a = -20 ~ 0°C	2.2	-	V _{CC}	2.2	-	V _{CC}	2.2	-	V _{CC}		
	\overline{RES}	4.0	-	V _{CC}	4.0	-	V _{CC}	4.0	-	V _{CC}			
Input "Low" Voltage	V _{IL}		-0.3	-	0.8	-0.3	-	0.8	-0.3	-	0.8	V	
Input Leakage Current	Except EXTAL, XTAL	I _{in}	V _{in} =0~5.25V, V _{CC} =max	-2.5	-	2.5	-2.5	-	2.5	-2.5	-	2.5	μA
Three State (Off State) Input Current	D ₀ ~D ₇	I _{TSI}	V _{in} =0.4~2.4V, V _{CC} =max	-10	-	10	-10	-	10	-10	-	10	μA
	A ₀ ~A ₁₅ , R/W		-100	-	100	-100	-	100	-100	-	100		
Output "High" Voltage	D ₀ ~D ₇	V _{OH}	I _{LOAD} =-205μA, V _{CC} =min	2.4	-	-	2.4	-	-	2.4	-	-	V
	A ₀ ~A ₁₅ , R/W, Q, E		I _{LOAD} =-145μA, V _{CC} =min	2.4	-	-	2.4	-	-	2.4	-	-	
	BA, BS		I _{LOAD} =-100μA, V _{CC} =min	2.4	-	-	2.4	-	-	2.4	-	-	
Output "Low" Voltage	V _{OL}	I _{LOAD} =2mA	-	-	0.5	-	-	0.5	-	-	0.5	V	
Power Dissipation	P _D		-	-	1.0	-	-	1.0	-	-	1.0	W	
Input Capacitance	D ₀ ~D ₇	C _{in}	V _{in} =0V, T _a =25°C, f=1MHz	-	10	15	-	10	15	-	10	15	pF
	Except D ₀ ~D ₇		-	7	10	-	7	10	-	7	10		
Output Capacitance	A ₀ ~A ₁₅ , R/W, BA, BS	C _{out}		-	-	12	-	-	12	-	-	12	pF

*T_a=25°C, V_{CC}=5V

● AC CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = -20~+75°C, unless otherwise noted.)

1. CLOCK TIMING

Item	Symbol	Test Condition	HD6809			HD68A09			HD68B09			Unit
			min	typ	max	min	typ	max	min	typ	max	
Frequency of Operation (Crystal or External Input)	f _{X TAL}	Fig. 2, Fig. 3	0.4	—	4	0.4	—	6	0.4	—	8	MHz
Cycle Time	t _{cy c}		1000	—	10000	667	—	10000	500	—	10000	ns
Total Up Time	t _{UT}		975	—	—	640	—	—	480	—	—	ns
Processor Clock "High"	t _{PWEH}		450	—	15500	280	—	15700	220	—	15700	ns
Processor Clock "Low"	t _{PWEL}		430	—	6000	280	—	5000	210	—	5000	ns
E Rise and Fall Time	t _{Er} , t _{Ef}		—	—	25	—	—	25	—	—	20	ns
E _{Low} to Q _{High} Time	t _{AVS}		200	—	250	130	—	165	80	—	125	ns
Q Clock "High"	t _{PWQH}		450	—	5000	280	—	5000	220	—	5000	ns
Q Clock "Low"	t _{PWQL}		450	—	15500	280	—	15700	220	—	15700	ns
Q Rise and Fall Time	t _{Qr} , t _{Qf}		—	—	25	—	—	25	—	—	20	ns
Q _{Low} to E Falling	t _{QE}		200	—	—	133	—	—	100	—	—	ns

2. BUS TIMING

Item	Symbol	Test Condition	HD6809			HD68A09			HD68B09			Unit	
			min	typ	max	min	typ	max	min	typ	max		
Address Delay	t _{AD}	Fig. 2, Fig. 3	—	—	200	—	—	140	—	—	110	ns	
Address Valid to Q _{High}	t _{AQ}		50	—	—	25	—	—	15	—	—	ns	
Peripheral Read Access Time (t _{UT} - t _{AD} - t _{DSR} + t _{ACC})	t _{ACC}		695	—	—	440	—	—	330	—	—	ns	
Data Set Up Time (Read)	t _{DSR}		80	—	—	60	—	—	40	—	—	ns	
Input Data Hold Time	t _{DHR}	Fig. 2, Fig. 3 T _a = 0~+75°C	10	—	—	10	—	—	10	—	—	ns	
Address Hold Time	t _{AH}		Fig. 2, Fig. 3 T _a = -20~0°C	20	—	—	20	—	—	20	—	—	ns
				10	—	—	10	—	—	10	—	—	ns
Data Delay Time (Write)	t _{DDW}	Fig. 3	—	—	200	—	—	140	—	—	110	ns	
Output Hold Time	t _{DHW}	Fig. 3 T _a = 0~+75°C	30	—	—	30	—	—	30	—	—	ns	
		Fig. 3 T _a = -20~0°C	20	—	—	20	—	—	20	—	—	ns	

3. PROCESSOR CONTROL TIMING

Item	Symbol	Test Condition	HD6809			HD68A09			HD68B09			Unit
			min	typ	max	min	typ	max	min	typ	max	
MRDY Set Up Time	t _{PCSM}	Fig. 6~Fig. 10 Fig. 14, Fig. 15	125	—	—	125	—	—	110	—	—	ns
Interrupts Set Up Time	t _{PCS}		200	—	—	140	—	—	110	—	—	ns
HALT Set Up Time	t _{PCSH}		200	—	—	140	—	—	110	—	—	ns
RES Set Up Time	t _{PCSR}		200	—	—	140	—	—	110	—	—	ns
DMA/BREQ Set Up Time	t _{PCSD}		125	—	—	125	—	—	110	—	—	ns
Processor Control Rise and Fall Time	t _{PCR} , t _{PCF}		—	—	100	—	—	100	—	—	100	ns
Crystal Oscillator Start Time	t _{RC}		—	—	50	—	—	30	—	—	30	ms

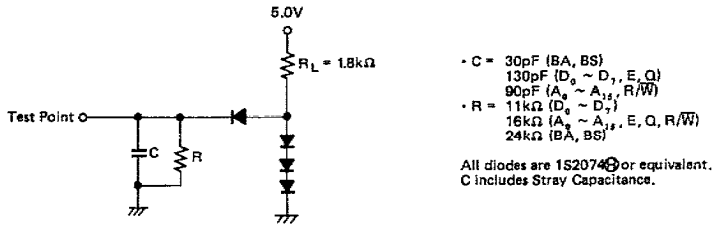


Figure 1 Bus Timing Test Load

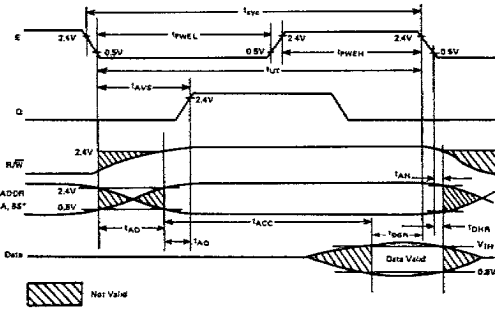


Figure 2 Read Data from Memory or Peripherals

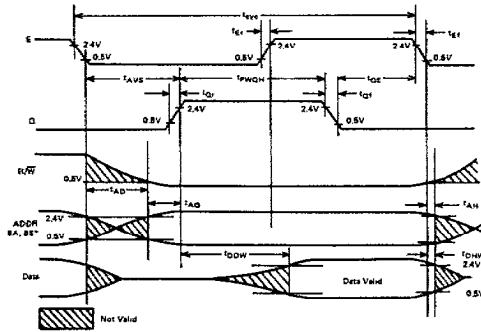


Figure 3 Write Data to Memory or Peripherals

PROGRAMMING MODEL

As shown in Figure 4, the HD6809 adds three registers to the set available in the HD6800. The added registers include a Direct Page Register, the User Stack pointer and a second Index Register.

Accumulators (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D

register, and is formed with the A register as the most significant byte.

Direct Page Register (DP)

The Direct Page Register of the HD6809 serves to enhance the Direct Addressing Mode. The content of this register appears at the higher address outputs (A₈ ~ A₁₅) during Direct Addressing Instruction execution. This allows the direct mode to be used at any place in memory, under program control. To ensure HD6800 compatibility, all bits of this register are cleared during Processor Reset.

● **Index Registers (X, Y)**

The Index Registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register

offset. During some indexed modes, the contents of the index register are incremented or decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

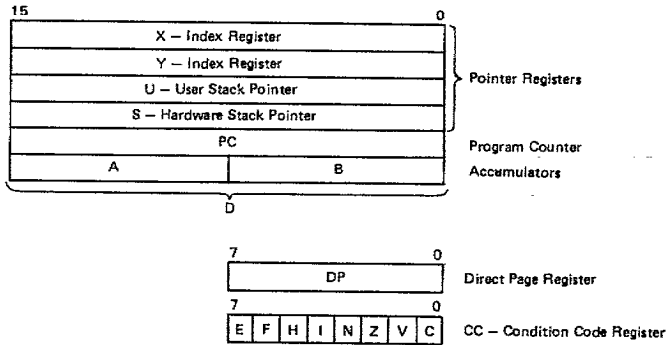


Figure 4 Programming Model of The Microprocessing Unit

● **Stack Pointer (U, S)**

The Hardware Stack Pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the HD6809 point to the top of the stack, in contrast to the HD6800 stack pointer, which pointed to the next free location on the stack. The User Stack Pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. Both Stack Pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support Push and Pull instructions. This allows the HD6809 to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

● **Program Counter**

The Program Counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative Addressing is provided allowing the Program Counter to be used like an index register in some situations.

● **Condition Code Register**

The Condition Code Register defines the State of the Processor at any given time. See Fig. 5.

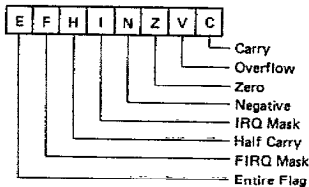


Figure 5 Condition Code Register Format

■ **CONDITION CODE REGISTER DESCRIPTION**

● **Bit 0 (C)**

Bit 0 is the carry flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract like instructions (CMP, NEG, SUB, SBC) and is the complement of the carry from the binary ALU.

● **Bit 1 (V)**

Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

● **Bit 2 (Z)**

Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.

● **Bit 3 (N)**

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to a one.

● **Bit 4 (I)**

Bit 4 is the \overline{IRQ} mask bit. The processor will not recognize interrupts from the \overline{IRQ} line if this bit is set to a one. \overline{NMI} , \overline{FIRQ} , \overline{IRQ} , \overline{RES} , and \overline{SWI} all are set 1 to a one; $\overline{SWI2}$ and $\overline{SWI3}$ do not affect I.

● **Bit 5 (H)**

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is

undefined in all subtract-like instructions.

● **Bit 6 (F)**

Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{FIRQ}}$ line if this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{SWI}}$, and $\overline{\text{RES}}$ all set F to a one. $\overline{\text{IRQ}}$, $\overline{\text{SWI2}}$ and $\overline{\text{SWI3}}$ do not affect F.

● **Bit 7 (E)**

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the stacked CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the Condition Code Register represents past action.

■ **SIGNAL DESCRIPTION**

● **Power (V_{SS} , V_{CC})**

Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is +5.0V $\pm 5\%$.

● **Address Bus ($A_0 \sim A_{15}$)**

Sixteen pins are used to output address information from the MPU onto the Address Bus. When the processor does not require the bus for a data transfer, it will output address $\overline{\text{FFFF}}_{16}$, $\overline{\text{R}/\overline{\text{W}}} = \text{"High"}$, and $\overline{\text{BS}} = \text{"Low"}$; this is a "dummy access" or $\overline{\text{VMA}}$ cycle. Addresses are valid on the rising edge of Q (see Figs. 2 and 3). All address bus drivers are made high impedance when output Bus Available (BA) is "High". Each pin will drive one Schottky TTL load or four LS TTL loads, and typically 90 pF.

● **Data Bus ($D_0 \sim D_7$)**

These eight pins provide communication with the system bi-directional data bus. Each pin will drive one Schottky TTL load or four LS TTL loads, and typically 130 pF.

● **Read/Write ($\overline{\text{R}/\overline{\text{W}}}$)**

This signal indicates the direction of data transfer on the data bus. A "Low" indicates that the MPU is writing data onto the data bus. $\overline{\text{R}/\overline{\text{W}}}$ is made high impedance when BA is "High". $\overline{\text{R}/\overline{\text{W}}}$ is valid on the rising edge of Q. Refer to Figs. 2 and 3.

● **Reset ($\overline{\text{RES}}$)**

A "Low" level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU, as shown in Fig. 6. The Reset vectors are fetched from locations $\overline{\text{FFFE}}_{16}$ and $\overline{\text{FFFF}}_{16}$ (Table 1) when Interrupt Acknowledge is true, ($\overline{\text{BA}} \cdot \overline{\text{BS}} = 1$). During initial power-on, the Reset line should be held "Low" until the clock oscillator is fully operational. See Fig. 7.

Because the HD6809 Reset pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage ensures that all peripherals are out of the reset state before the Processor.

Table 1 Memory Map for Interrupt Vectors

Memory Map For Vector Locations		Interrupt Vector Description
MS	LS	
FFFE	FFFF	$\overline{\text{RES}}$
FFFC	FFFD	$\overline{\text{NMI}}$
FFFA	FFFB	$\overline{\text{SWI}}$
FFF8	FFF9	$\overline{\text{IRQ}}$
FFF6	FFF7	$\overline{\text{FIRQ}}$
FFF4	FFF5	$\overline{\text{SWI2}}$
FFF2	FFF3	$\overline{\text{SWI3}}$
FFF0	FFF1	Reserved

● **$\overline{\text{HALT}}$**

A "Low" level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When halted, the BA output is driven "High" indicating the buses are high impedance. BS is also "High" which indicates the processor is in the Halt or Bus Grant state. While halted, the MPU will not respond to external real-time requests ($\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$) although $\overline{\text{DMA/BREQ}}$ will always be accepted, and $\overline{\text{NMI}}$ or $\overline{\text{RES}}$ will be latched for later response. During the Halt state Q and E continue to run normally. If the MPU is not running ($\overline{\text{RES}}$, $\overline{\text{DMA/BREQ}}$), a halted state ($\overline{\text{BA}} \cdot \overline{\text{BS}} = 1$) can be achieved by pulling $\overline{\text{HALT}}$ "Low" while $\overline{\text{RES}}$ is still "Low". If $\overline{\text{DMA/BREQ}}$ and $\overline{\text{HALT}}$ are both pulled "Low", the processor will reach the last cycle of the instruction (by reverse cycle stealing) where the machine will then become halted. See Figs. 8 and 16.

● **Bus Available, Bus Status ($\overline{\text{BA}}$, $\overline{\text{BS}}$)**

The BA output is an indication of an internal control signal which makes the MOS buses of the MPU high impedance. This signal does not imply that the bus will be available for more than one cycle. When BA goes "Low", an additional dead cycle will elapse before the MPU acquires the bus.

The BS output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q).

Table 2 MPU State Definition

BA	BS	MPU State
0	0	Normal (Running)
0	1	Interrupt or RESET Acknowledge
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant

Interrupt Acknowledge is indicated during both cycles of a hardware-vector-fetch ($\overline{\text{RES}}$, $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{SWI}}$, $\overline{\text{SWI2}}$, $\overline{\text{SWI3}}$). This signal, plus decoding of the lower four address lines, can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device. See Table 1.

Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

Halt/Bus Grant is true when the HD6809 is in a Halt or Bus Grant condition.

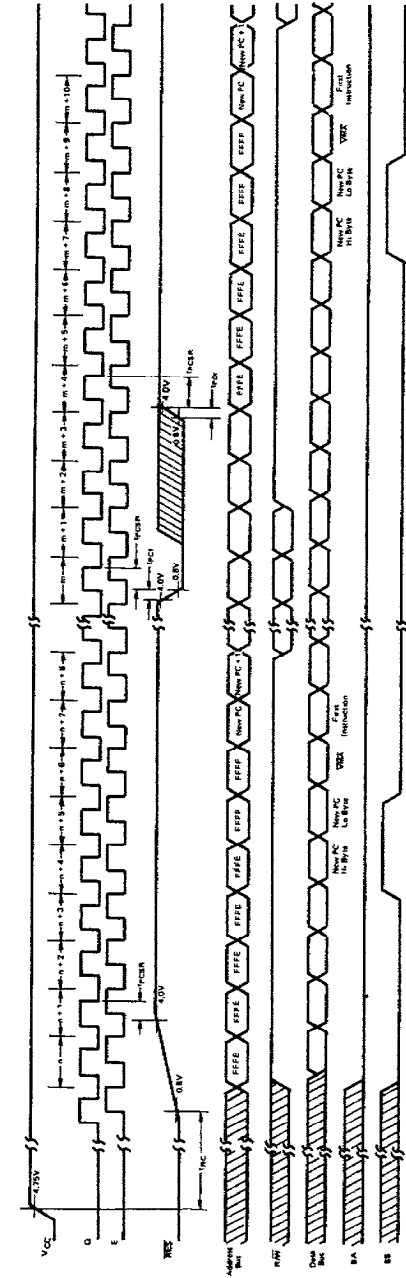


Figure 6 RES Timing

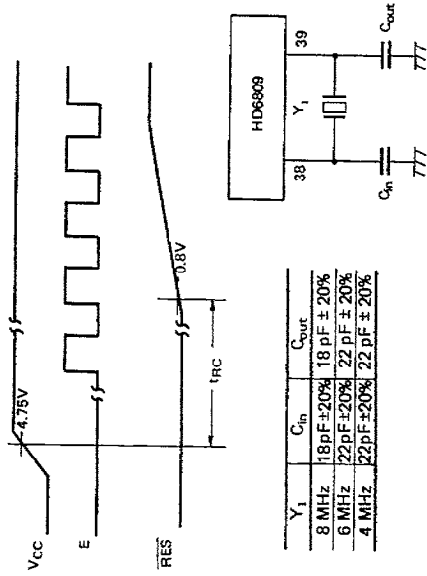


Figure 7 Crystal Connections and Oscillator Start Up

• **Non Maskable Interrupt (NMI)***

A negative edge on this input requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program, and also has a higher priority than FIRQ, IRQ or software interrupts. During recognition of an NMI, the entire machine state is saved on the

hardware stack. After reset, an NMI will not be recognized until the first program load of the Hardware Stack Pointer (S). The pulse width of NMI "Low" must be at least one E cycle. If the NMI input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Fig. 9.

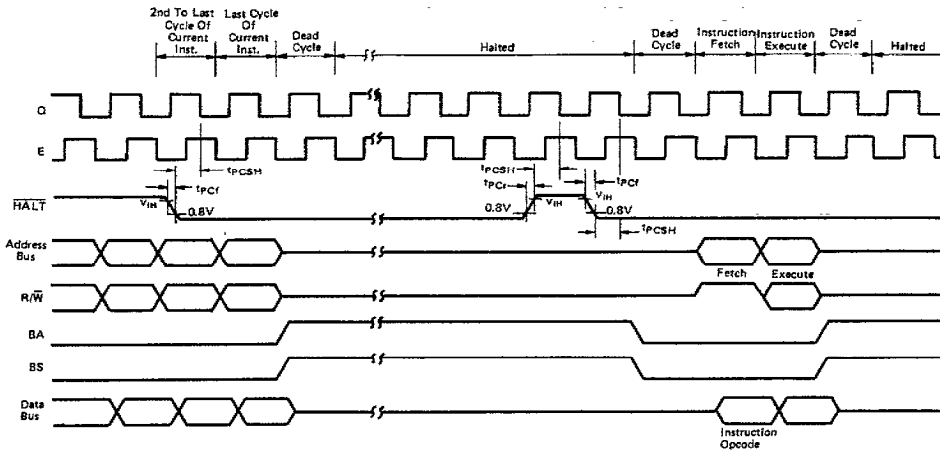


Figure 8 HALT and Single Instruction Execution for System Debug

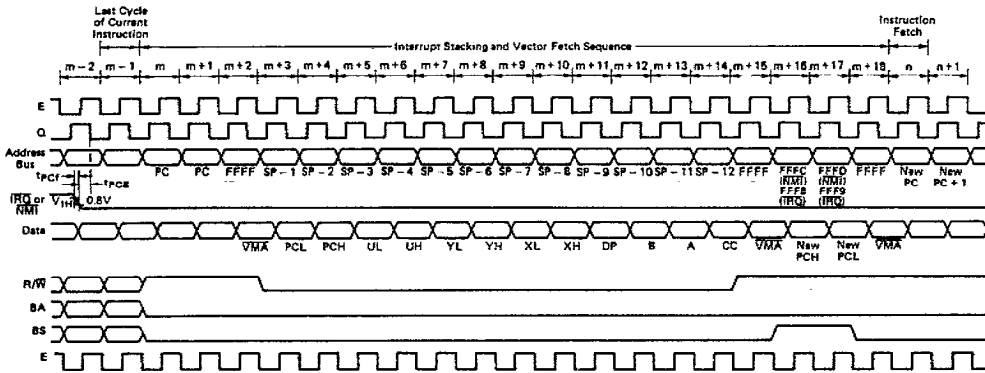


Figure 9 IRQ and NMI Interrupt Timing

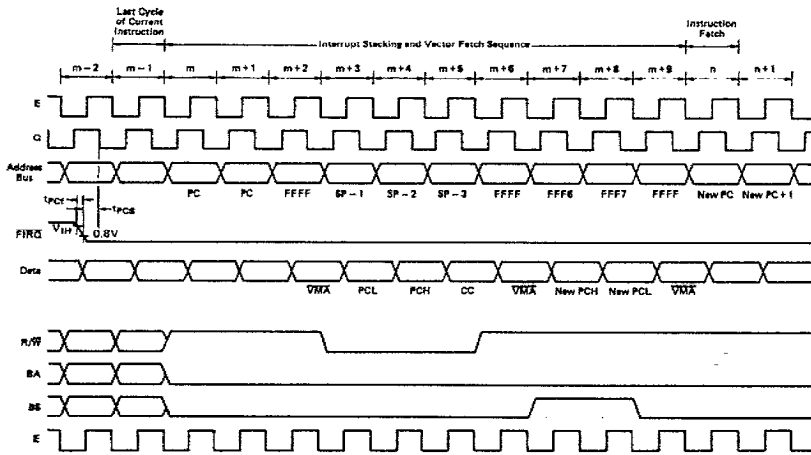


Figure 10 $\overline{\text{FIRQ}}$ Interrupt Timing

● **Fast-Interrupt Request ($\overline{\text{FIRQ}}$)***

A "Low" level on this input pin will initiate a fast interrupt sequence provided its mask bit (F) in the CC is clear. This sequence has priority over the standard Interrupt Request ($\overline{\text{IRQ}}$), and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Fig. 10.

● **Interrupt Request ($\overline{\text{IRQ}}$)***

A "Low" level input on this pin will initiate an interrupt Request sequence provided the mask bit (I) in the CC is clear. Since $\overline{\text{IRQ}}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{\text{FIRQ}}$. $\overline{\text{IRQ}}$ also has a lower priority than $\overline{\text{FIRQ}}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Fig. 9.

* $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, and $\overline{\text{IRQ}}$ requests are sampled on the falling edge of Q. One cycle is required for synchronization before these interrupts are recognized. The pending interrupt(s) will not be serviced until completion of the current instruction unless a SYNC or CWAI condition is present. If $\overline{\text{IRQ}}$ and $\overline{\text{FIRQ}}$ do not remain "Low" until completion of the current instruction they may not be recognized. However, $\overline{\text{NMI}}$ is latched and need only remain "Low" for one cycle.

● **XTAL, EXTAL**

These inputs are used to connect the on-chip oscillator to an external parallel-resonant crystal. Alternately, the pin EXTAL may be used as a TTL level input for external timing by grounding XTAL. The crystal or external frequency is four times the bus frequency. See Fig. 7. Proper RF layout techniques should be observed in the layout of printed circuit boards.

< NOTE FOR BOARD DESIGN OF THE OSCILLATION CIRCUIT >

In designing the board, the following notes should be taken when the crystal oscillator is used.

- 1) Crystal oscillator and load capacity C_{in} , C_{out} must be placed

near the LSI as much as possible.

[Normal oscillation may be disturbed when external noise is induced to pin 38 and 39.]

- 2) Pin 38 and 39 signal line should be wired apart from other signal line as much as possible. Don't wire them in parallel.

[Normal oscillation may be disturbed when E or Q signal is feedbacked to pin 38 and 39.]

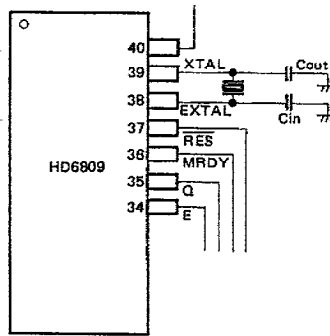
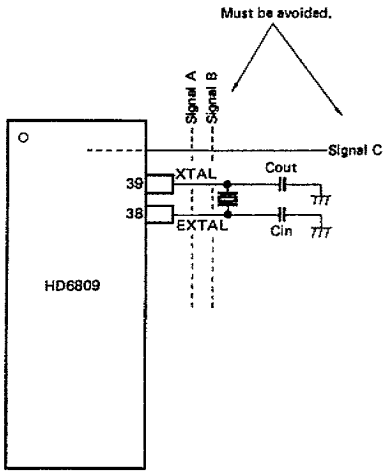


Figure 11 Board Design of the Oscillation Circuit.

< THE FOLLOWING DESIGN MUST BE AVOIDED >

A signal line or a power source line must not cross or go near the oscillation circuit line as shown in Fig. 12 to prevent the induction from these lines and perform the correct oscillation. The resistance among XTAL, EXTAL and other pins should be over 10M Ω .



• E, Q

E is similar to the HD6800 bus timing signal ϕ_2 ; Q is a quadrature clock signal which leads E. Q has no parallel on the HD6800. Addresses from the MPU will be valid with the leading edge of Q. Data is latched on the falling edge of E. Timing for E and Q is shown in Fig. 13.

• MRDY

This input control signal allows stretching of E and Q to extend data-access time. E and Q operate normally while MRDY is "High". When MRDY is "Low", E and Q may be stretched in integral multiples of quarter (1/4) bus cycles, thus allowing interface to slow memories, as shown in Fig. 14. A maximum

Figure 12 Example of Normal Oscillation may be Disturbed.

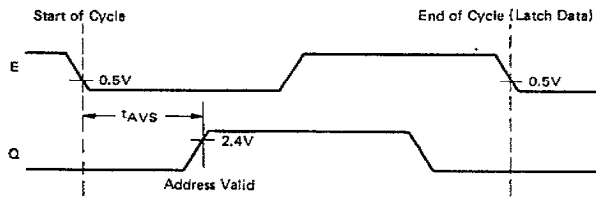


Figure 13 E/Q Relationship

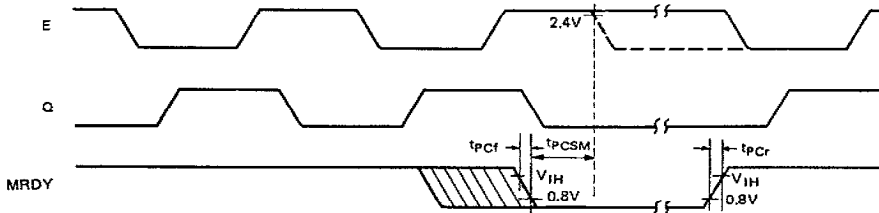


Figure 14 MRDY Timing

stretch is 10 microseconds. During nonvalid memory access (VMA cycles) MRDY has no effect on stretching E and Q; this inhibits slowing the processor during "don't care" bus accesses. MRDY may also be used to stretch clocks (for slow memory) when bus control has been transferred to an external device (through the use of HALT and DMA/BREQ). Also MRDY has effect on stretching E and Q during Dead Cycle.

● **DMA/BREQ**

The DMA/BREQ input provides a method of suspending execution and acquiring the MPU bus for another use, as shown in Fig. 15. Typical uses include DMA and dynamic memory refresh.

Transition of DMA/BREQ should occur during Q. A "Low" level on this pin will stop instruction execution at the end of the current cycle. The MPU will acknowledge DMA/BREQ by setting BA and BS to "High" level. The requesting device will now have up to 15 bus cycles before the MPU retrieves the bus for self-refresh. Self-refresh requires one bus cycle with a lead-

ing and trailing dead cycle. See Fig. 16.

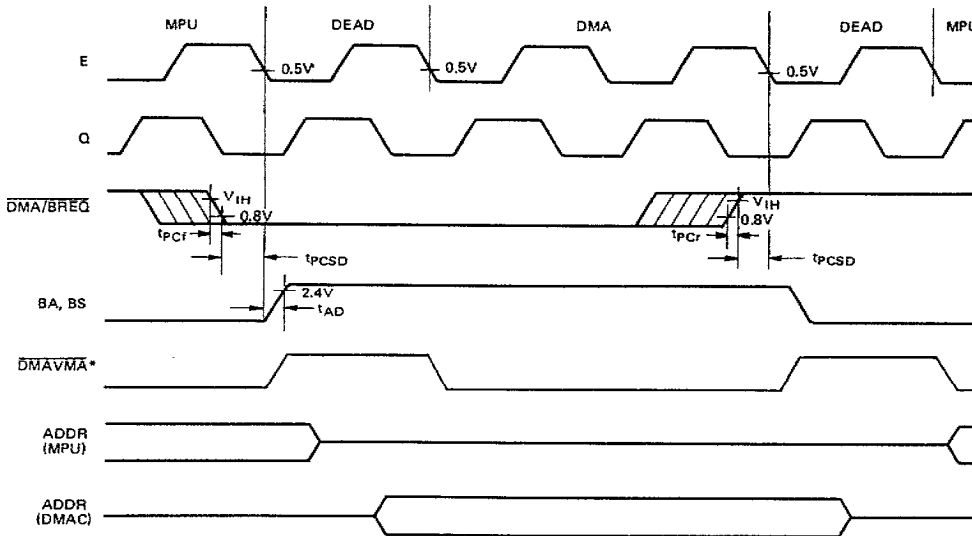
Typically, the DMA controller will request to use the bus by asserting DMA/BREQ pin "Low" on the leading edge of E. When the MPU replies by setting BA and BS to a one, that cycle will be a dead cycle used to transfer bus mastership to the DMA controller.

False memory accesses may be prevented during and dead cycles by developing a system DMAVMA signal which is "Low" in any cycle when BA has changed.

When BA goes "Low" (either as a result of DMA/BREQ = "High" or MPU self-refresh), the DMA device should be taken off the bus. Another dead cycle will elapse before the MPU accesses memory, to allow transfer of bus mastership without contention.

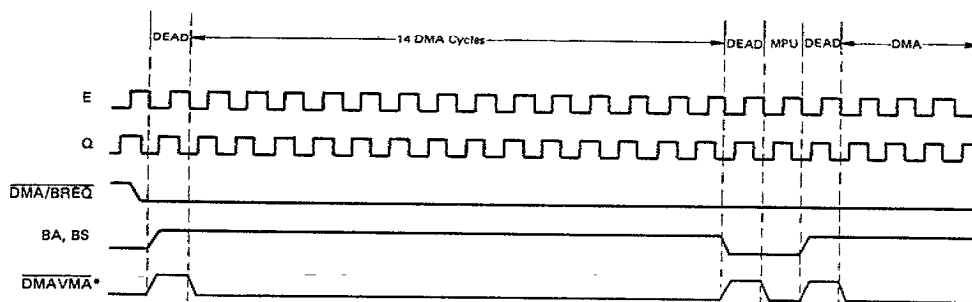
■ **MPU OPERATION**

During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This



*DMAVMA is a signal which is developed externally, but is a system requirement for DMA.

Figure 15 Typical DMA Timing (<14 Cycles)



*DMAVMA is a signal which is developed externally, but is a system requirement for DMA.

Figure 16 Auto-Refresh DMA Timing (Reverse Cycle Stealing)

sequence begins at RES and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter normal MPU operation are: SWI, SWI2, SWI3, CWAI, RTI and SYNC. An interrupt, HALT or DMA/BREQ can also alter the normal execution of instructions. Fig. 17 illustrates the flow chart for the HD6809.

■ ADDRESSING MODES

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The HD6809 has the most complete set of addressing modes available on any microcomputer today. For example, the HD6809 has 59 basic instructions; however, it recognizes 1464 different variations of instructions and addressing modes. The addressing modes support modern programming techniques. The following addressing modes are available on the HD6809:

- (1) Implied (Includes Accumulator)
- (2) Immediate
- (3) Extended
- (4) Extended Indirect
- (5) Direct
- (6) Register
- (7) Indexed
 - Zero-Offset
 - Constant Offset
 - Accumulator Offset
 - Auto Increment/Decrement
- (8) Indexed Indirect
- (9) Relative
- (10) Program Counter Relative

● Implied (Includes Accumulator)

In this addressing mode, the opcode of the instruction contains all the address information necessary. Examples of Implied Addressing are: ABX, DAA, SWI, ASRA, and CLRB.

● Immediate Addressing

In Immediate Addressing, the effective address of the data is the location immediately following the opcode (i.e., the data to be used in the instruction immediately follows the opcode of the instruction). The HD6809 uses both 8 and 16-bit immediate values depending on the size of argument specified by the opcode. Examples of instructions with Immediate Addressing are:

```
LDA #$20
LDX #$F000
LDY #CAT
```

(NOTE) # signifies Immediate addressing, S signifies hexadecimal value.

● Extended Addressing

In Extended Addressing, the contents of the two bytes immediately following the opcode fully specify the 16-bit effective address used by the instruction. Note that the address generated by an extended instruction defines an absolute address and is not position independent. Examples of Extended Addressing include:

```
LDA CAT
STX MOUSE
LDD $2000
```

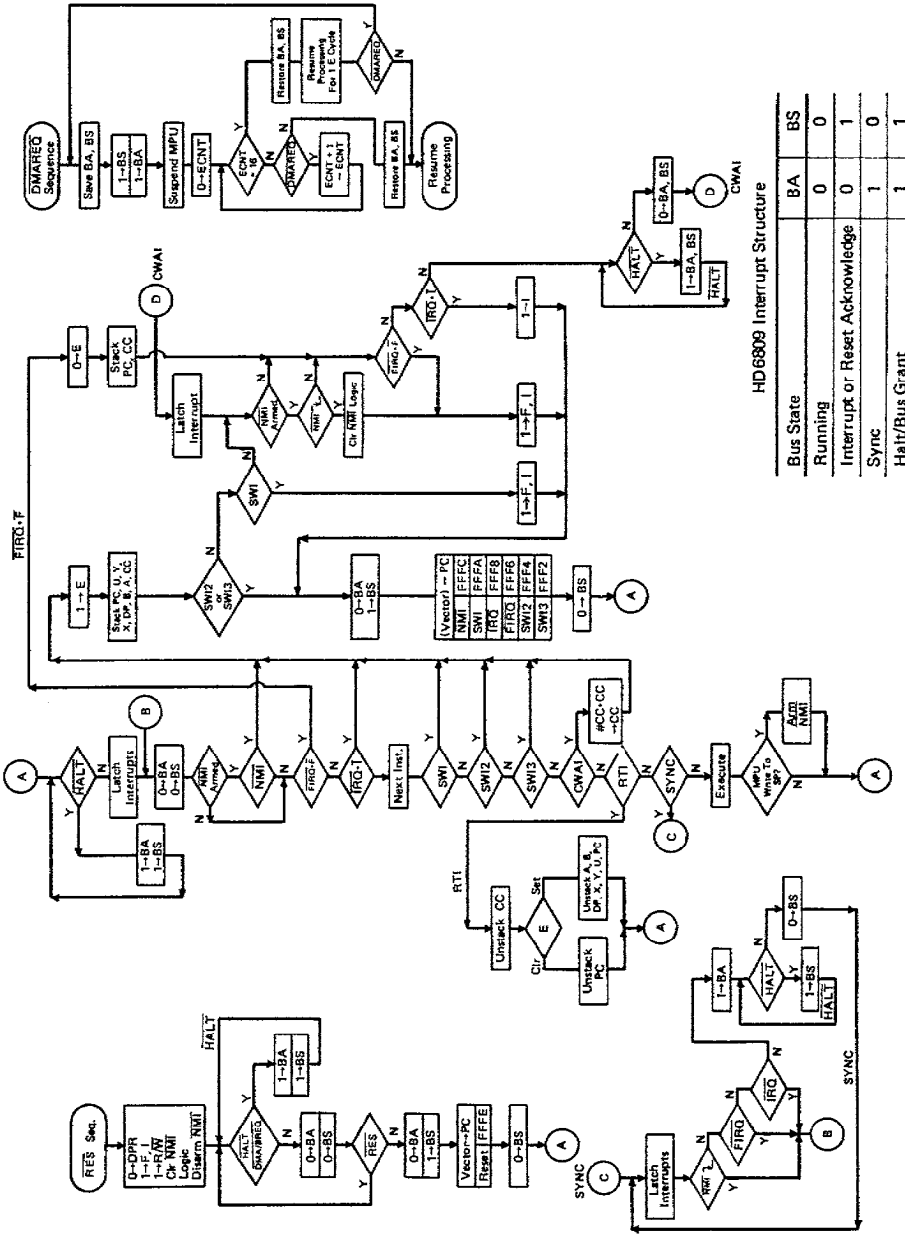
● Extended Indirect

As a special case of indexed addressing (discussed below), "1" level of indirection may be added to Extended Addressing. In Extended Indirect, the two bytes following the postbyte of an Indexed instruction contain the address of the data.

```
LDA [CAT]
LDX [$FFFE]
STU [DOG]
```

● Direct Addressing

Direct addressing is similar to extended addressing except that only one byte of address follows the opcode. This byte specifies the lower 8-bit of the address to be used. The upper 8-bit of the address are supplied by the direct page register. Since only one byte of address is required in direct addressing, this mode requires less memory and executes faster than extended addressing. Of course, only 256 locations (one page) can be



HD6809 Interrupt Structure

Bus State	BA	BS
Running	0	0
Interrupt or Reset Acknowledge	0	1
Sync	1	0
Halt/Bus Grant	1	1

(NOTE) Asserting RES will result in entering the reset sequence from any point in the flow chart.

Figure 17 Flowchart for HD6809 Instruction

accessed without redefining the contents of the DP register. Since the DP register is set to \$00 on Reset, direct addressing on the HD6809 is compatible with direct addressing on the HD6800. Indirection is not allowed in direct addressing. Some examples of direct addressing are:

```
LDA    $30
SETDP  $10 (Assembler directive)
LDB    $1030
LDD    <CAT
```

(NOTE) < is an assembler directive which forces direct addressing.

● Register Addressing

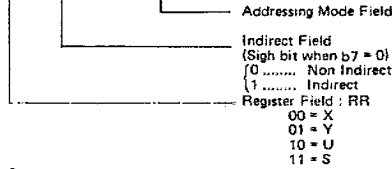
Some opcodes are followed by a byte that defines a register or set of registers to be used by the instruction. This is called a postbyte. Some examples of register addressing are:

```
TFR    X, Y    Transfers X into Y
EXG    A, B    Exchanges A with B
PSHS   A, B, X, Y  Push Y, X, B and A onto S
PULU   X, Y, D  Pull D, X, and Y from U
```

● Indexed Addressing

In all indexed addressing, one of the pointer registers (X, Y, U, S, and sometimes PC) is used in a calculation of the effective address of the operand to be used by the instruction. Five basic types of indexing are available and are discussed below. The postbyte of an indexed instruction specifies the basic type and variation of the addressing mode as well as the pointer register to be used. Fig. 18 lists the legal formats for the postbyte. Table 3 gives the assembler form and the number of cycles and bytes

Post-Byte Register Bit								Indexed Addressing Mode
7	6	5	4	3	2	1	0	
0	R	R	x	x	x	x	x	EA = ,R + 5 Bit Offset
1	R	R	0	0	0	0	0	,R +
1	R	R	0/1	0	0	0	1	,R ++
1	R	R	0	0	0	1	0	,-R
1	R	R	0/1	0	0	1	1	,--R
1	R	R	0/1	0	1	0	0	EA = ,R + 0 Offset
1	R	R	0/1	0	1	0	1	EA = ,R + ACCB Offset
1	R	R	0/1	0	1	1	0	EA = ,R + ACCA Offset
1	R	R	0/1	1	0	0	0	EA = ,R + 8 Bit Offset
1	R	R	0/1	1	0	0	1	EA = ,R + 16 Bit Offset
1	R	R	0/1	1	0	1	1	EA = ,R + D Offset
1	x	x	0/1	1	1	0	0	EA = ,PC + 8 Bit Offset
1	x	x	0/1	1	1	0	1	EA = ,PC + 16 Bit Offset
1	R	R	1	1	1	1	1	EA = [,Address]



x = Don't Care

Figure 18 Index Addressing Postbyte Register Bit Assignments

Table 3 Indexed Addressing Mode

Type	Forms	Non Indirect			Indirect		
		Assembler Form	Postbyte OP Code	+ ~ #	Assembler Form	Postbyte OP Code	+ ~ #
Constant Offset From R (2's Complement Offsets)	No Offset	,R	1RR00100	0 0	[,R]	1RR10100	3 0
	5 Bit Offset	n, R	0RRnnnnn	1 0	defaults to 8-bit		
	8 Bit Offset	n, R	1RR01000	1 1	[n, R]	1RR11000	4 1
	16 Bit Offset	n, R	1RR01001	4 2	[n, R]	1RR11001	7 2
Accumulator Offset From R (2's Complement Offsets)	A Register Offset	A, R	1RR00110	1 0	[A, R]	1RR10110	4 0
	B Register Offset	B, R	1RR00101	1 0	[B, R]	1RR10101	4 0
	D Register Offset	D, R	1RR01011	4 0	[D, R]	1RR11011	7 0
Auto Increment/Decrement R	Increment By 1	,R +	1RR00000	2 0	not allowed		
	Increment By 2	,R ++	1RR00001	3 0	[,R ++]	1RR10001	6 0
	Decrement By 1	,-R	1RR00010	2 0	not allowed		
	Decrement By 2	,--R	1RR00011	3 0	[,--R]	1RR10011	6 0
Constant Offset From PC (2's Complement Offsets)	8 Bit Offset	n, PCR	1xx01100	1 1	[n, PCR]	1xx11100	4 1
	16 Bit Offset	n, PCR	1xx01101	5 2	[n, PCR]	1xx11101	8 2
Extended Indirect	16 Bit Address	-	-	-	[n]	10011111	5 2

R = X, Y, U or S RR:
 x = Don't Care 00 = X
 01 = Y
 10 = U
 11 = S

+ and # indicate the number of additional cycles and bytes for the particular variation.

added to the basic values for indexed addressing for each variation.

Zero-Offset Indexed

In this mode, the selected pointer register contains the effective address of the data to be used by the instruction. This is the fastest indexing mode.

Examples are:
 LDD 0,X
 LDA S

Constant Offset Indexed

In this mode, a two's-complement offset and the contents of one of the pointer registers are added to form the effective address of the operand. The pointer register's initial content is unchanged by the addition.

Three sizes of offsets are available:
 5-bit (-16 to +15)
 8-bit (-128 to +127)
 16-bit (-32768 to +32767)

The two's complement 5-bit offset is included in the postbyte and, therefore, is most efficient in use of bytes and cycles. The two's complement 8-bit offset is contained in a single byte following the postbyte. The two's complement 16-bit offset is in the two bytes following the postbyte. In most cases the programmer need not be concerned with the size of this offset since the assembler will select the optimal size automatically.

Examples of constant-offset indexing are:
 LDA 23,X
 LDX -2,S
 LDY 300,X
 LDU CAT,Y

Accumulator-Offset Indexed

This mode is similar to constant offset indexed except that the two's-complement value in one of the accumulators (A, B or D) and the contents of one of the pointer registers are added to form the effective address of the operand. The contents of both the accumulator and the pointer register are unchanged by the addition. The postbyte specifies which accumulator to use as an offset and no additional bytes are required. The advantage of an accumulator offset is that the value of the offset can be calculated by a program at run-time.

Some examples are:
 LDA B,Y
 LDX D,Y
 LEAX B,X

Auto Increment/Decrement Indexed

In the auto increment addressing mode, the pointer register contains the address of the operand. Then, after the pointer register is used it is incremented by one or two. This addressing mode is useful in stepping through tables, moving data, or for the creation of software stacks. In auto decrement, the pointer register is decremented prior to use as the address of the data. The use of auto decrement is similar to that of auto increment; but the tables, etc., are scanned from the "High" to "Low" addresses. The size of the increment/decrement can be either one or two to allow for tables of either 8 or 16-bit data to be accessed and is selectable by the programmer. The pre-decrement, post-increment nature of these modes allow them to be used to create additional software stacks that behave identically to the U and S stacks.

Some examples of the auto increment/decrement addressing modes are:

LDA ,X+
 STD ,Y+
 LDB ,-Y
 LDX ,--S

Care should be taken in performing operations on 16-bit pointer registers (X, Y, U, S) where the same register is used to calculate the effective address.

Consider the following instruction:

STX 0, X++ (X initialized to 0)

The desired result is to store a 0 in locations \$0000 and \$0001 then increment X to point to \$0002. In reality, the following occurs:

0 → temp calculate the EA; temp is a holding register
 X + 2 → X perform autoincrement
 X → (temp) do store operation

• **Indexed Indirect**

All of the indexing modes with the exception of auto increment/decrement by one, or a ±4-bit offset may have an additional level of indirection specified. In indirect addressing, the effective address is contained at the location specified by the contents of the Index register plus any offset. In the example below, the A accumulator is loaded indirectly using an effective address calculated from the Index register and an offset.

Before Execution
 A = ×× (don't care)
 X = \$F000
 \$0100 LDA [\$10,X] EA is now \$F010
 \$F010 \$F1 \$F150 is now the
 \$F011 \$50 new EA
 \$F150 SAA
 After Execution
 A = \$AA Actual Data Loaded
 X = \$F000

All modes of indexed indirect are included except those which are meaningless (e.g., auto increment/decrement by 1 indirect). Some examples of indexed indirect are:

LDA [,X]
 LDD [10,S]
 LDA [B,Y]
 LDD [,X+]

• **Relative Addressing**

The byte(s) following the branch opcode is (are) treated as a signed offset which may be added to the program counter. If the branch condition is true then the calculated address (PC + signed offset) is loaded into the program counter. Program execution continues at the new location as indicated by the PC; short (1 byte offset) and long (2 bytes offset) relative addressing modes are available. All of memory can be reached in long relative addressing as an effective address is interpreted modulo 2¹⁶. Some examples of relative addressing are:

	BEQ	CAT	(short)
	BGT	DOG	(short)
CAT	LBEQ	RAT	(long)
DOG	LBGT	RABBIT	(long)

•
•
•
RAT NOP
RABBIT NOP

● Program Counter Relative

The PC can be used as the pointer register with 8 or 16-bit signed offsets. As in relative addressing, the offset is added to the current PC to create the effective address. The effective address is then used as the address of the operand or data. Program Counter Relative Addressing is used for writing position independent programs. Tables related to a particular routine will maintain the same relationship after the routine is moved, if referenced relative to the Program Counter. Examples are:

```
LDA CAT, PCR
LEAX TABLE, PCR
```

Since program counter relative is a type of indexing, an additional level of indirection is available.

```
LDA [CAT, PCR]
LDU [DOG, PCR]
```

■ HD6809 INSTRUCTION SET

The instruction set of the HD6809 is similar to that of the HD6800 and is upward compatible at the source code level. The number of opcodes has been reduced from 72 to 59, but because of the expanded architecture and additional addressing modes, the number of available opcodes (with different addressing modes) has risen from 197 to 1464.

Some of the new instructions and addressing modes are described in detail below:

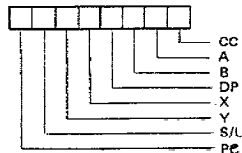
● PSHU/PSHS

The push instructions have the capability of pushing onto either the hardware stack (S) or user stack (U) any single register, or set of registers with a single instruction.

● PULU/PULS

The pull instructions have the same capability of the push instruction, in reverse order. The byte immediately following the push or pull opcode determines which register or registers are to be pushed or pulled. The actual PUSH/PULL sequence is fixed; each bit defines a unique register to push or pull, as shown in below.

PUSH/PULL POST BYTE



← Pull Order Push Order →

PC U Y X DP B A CC
 FFFF... ← increasing memory address0000
 PC S Y X DP B A CC

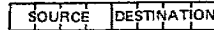
● TFR/EXG

Within the HD6809, any register may be transferred to or exchanged with another of like-size; i.e., 8-bit to 8-bit or 16-bit to 16-bit. Bits 4-7 of postbyte define the source register, while bits 0-3 represent the destination register. Three are denoted as follows:

0000 - D	0101 - PC
0001 - X	1000 - A *
0010 - Y	1001 - B
0011 - U	1010 - CC
0100 - S	1011 - DP

(NOTE) All other combinations are undefined and INVALID.

TRANSFER/EXCHANGE POST BYTE



● LEAX/LEAY/LEAU/LEAS

The LEA (Load Effective Address) works by calculating the effective address used in an indexed instruction and stores that address value, rather than the data at that address, in a pointer register. This makes all the features of the internal addressing hardware available to the programmer. Some of the implications of this instruction are illustrated in Table 4.

The LEA instruction also allows the user to access data in a position independent manner. For example:

```
LEAX MSG1, PCR
LBSR PDATA (Print message routine)
```

```
MSG1 FCC            'MESSAGE'
```

This sample program prints 'MESSAGE'. By writing MSG1, PCR, the assembler computes the distance between the present address and MSG1. This result is placed as a constant into the LEAX instruction which will be indexed from the PC value at the time of execution. No matter where the code is located, when it is executed, the computed offset from the PC will put the absolute address of MSG1 into the X pointer register. This code is totally position independent.

The LEA instructions are very powerful and use an internal holding register (temp). Care must be exercised when using the LEA instructions with the autoincrement and autodecrement addressing modes due to the sequence of internal operations. The LEA internal sequence is outlined as follows:

- LEAa, b+ (any of the 16-bit pointer registers X, Y, U or S may be substituted for a and b.)
1. b → temp (calculate the EA)
 2. b + 1 → b (modify b, postincrement)
 3. temp → a (load a)
- LEAa, -b
1. b - 1 → temp (calculate EA with predecrement)
 2. b - 1 → b (modify b, predecrement)
 3. temp → a (load a)

Autoincrement-by-two and autodecrement-by-two instructions work similarly. Note that LEAX, X+ does not change X, however LEAX, -X does decrement X. LEAX 1, X should be used to increment X by one.

Table 4 LEA Examples

Instruction	Operation	Comment
LEAX 10, X	X + 10 → X	Adds 5-bit constant 10 to X
LEAX 500, X	X + 500 → X	Adds 16-bit constant 500 to X
LEAY A, Y	Y + A → Y	Adds 8-bit accumulator to Y
LEAY D, Y	Y + D → Y	Adds 16-bit D accumulator to Y
LEAU -10, U	U - 10 → U	Subtracts 10 from U
LEAS -10, S	S - 10 → S	Used to reserve area on stack
LEAS 10, S	S + 10 → S	Used to 'clean up' stack
LEAX 5, S ₊	S + 5 → X	Transfers as well as adds

• MUL

Multiplies the unsigned binary numbers in the A and B accumulator and places the unsigned result into the 16-bit D accumulator. This unsigned multiply also allows multiple-precision multiplications.

Long And Short Relative Branches

The HD6809 has the capability of program counter relative branching throughout the entire memory map. In this mode, if the branch is to be taken, the 8 or 16-bit signed offset is added to the value of the program counter to be used as the effective address. This allows the program to branch anywhere in the 64k memory map. Position independent code can be easily generated through the use of relative branching. Both short (8-bit) and long (16-bit) branches are available.

• SYNC

After encountering a Sync instruction, the MPU enters a Sync state, stops processing instructions and waits for an interrupt. If the pending interrupt is non-maskable (NMI) or maskable (FIRQ, IRQ) with its mask bit (F or I) clear, the processor will clear the Sync state and perform the normal interrupt stacking and service routine. Since FIRQ and IRQ are not edge-triggered, a "Low" level with a minimum duration of three bus cycles is required to assure that the interrupt will be taken. If the pending interrupt is maskable (FIRQ, IRQ) with its mask bit (F or I) set, the processor will clear the Sync state and continue processing by executing the next inline instruction. Fig. 19 depicts Sync timing.

Software Interrupts

A Software Interrupt is an instruction which will cause an interrupt, and its associated vector fetch. These Software Interrupts are useful in operating system calls, software debugging, trace operations, memory mapping, and software development systems. Three levels of SWI are available on this HD6809, and are prioritized in the following order: SWI, SWI2, SWI3.

16-Bit Operation

The HD6809 has the capability of processing 16-bit data. These instructions include loads, stores, compares, adds, subtracts, transfers, exchanges, pushes and pulls.

■ CYCLE-BY-CYCLE OPERATION

The address bus cycle-by-cycle performance chart illustrates the memory-access sequence corresponding to each possible instruction and addressing mode in the HD6809. Each instruction begins with an opcode fetch. While that opcode is being internally decoded, the next program byte is always fetched. (Most instructions will use the next byte, so this technique considerably speeds throughput.) Next, the operation of each opcode will follow the flow chart. VMA is an indication of

FFFF₁₆ on the address bus, R/W="High" and BS="Low". The following examples illustrate the use of the chart; see Fig. 20.

Example 1: LBSR (Branch Taken)
Before Execution SP = F000

\$8000	LBSR	CAT
.	.	.
.	.	.
.	.	.
\$A000	CAT	.

CYCLE-BY-CYCLE FLOW

Cycle #	Address	Data	R/W	Description
1	8000	17	1	Opcode Fetch
2	8001	1F	1	Offset High Byte
3	8002	FD	1	Offset Low Byte
4	FFFF	*	1	VMA Cycle
5	FFFF	*	1	VMA Cycle
6	A000	*	1	Computed Branch Address
7	FFFF	*	1	VMA Cycle
8	FFFF	03	0	Stack Low Order Byte of Return Address
9	FFFF	80	0	Stack High Order Byte of Return Address

Example 2: DEC (Extended)

\$8000	DEC	\$A000
\$A000	FCB	\$80

CYCLE-BY-CYCLE FLOW

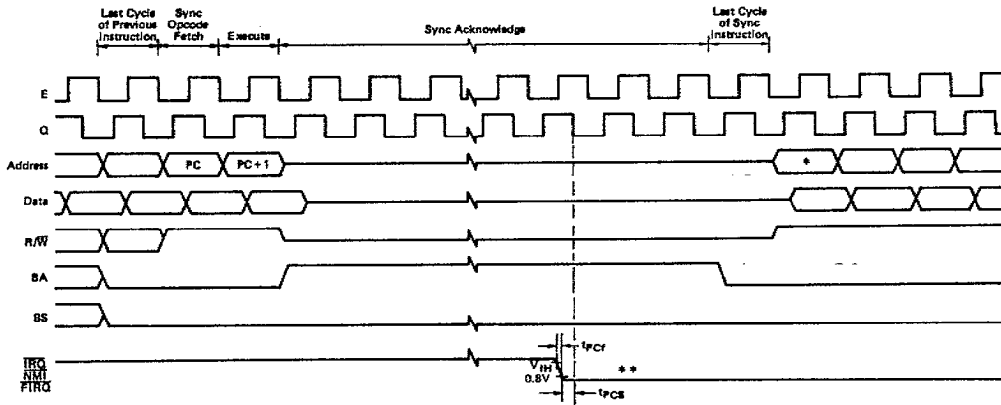
Cycle #	Address	Data	R/W	Description
1	8000	7A	1	Opcode Fetch
2	8001	A0	1	Operand Address, High Byte
3	8002	00	1	Operand Address, Low Byte
4	FFFF	*	1	VMA Cycle
5	A000	80	1	Read the Data
6	FFFF	*	1	VMA Cycle
7	A000	7F	0	Store the Decrement Data

* The data bus has the data at that particular address.

■ HD6809 INSTRUCTION SET TABLES

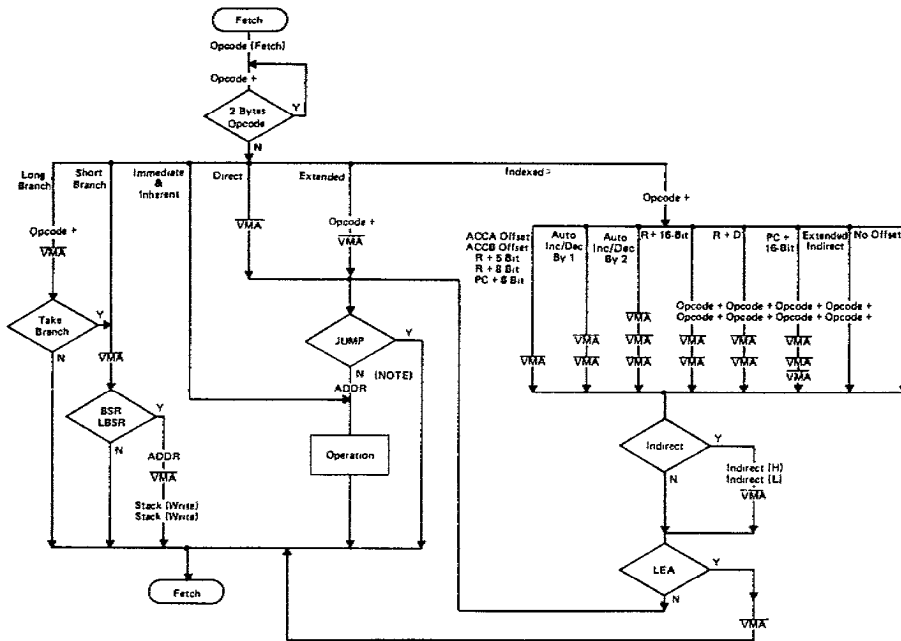
The instructions of the HD6809 have been broken down into five different categories. They are as follows:

- 8-Bit operation (Table 5)
 - 16-Bit operation (Table 6)
 - Index register/stack pointer instructions (Table 7)
 - Relative branches (long or short) (Table 8)
 - Miscellaneous instructions (Table 9)
- HD6809 instruction set tables and Hexadecimal Values of instructions are shown in Table 10 and Table 11.



- (NOTES) * If the associated mask bit is set when the interrupt is requested, this cycle will be an instruction fetch from address location PC + 1. However, if the interrupt is accepted (NMI or an unmasked FIRQ or IRQ) interrupt processing continues with this cycle as (m) on Figure 9 and 10 (Interrupt Timing).
 ** If mask bits are clear, IRQ and FIRQ must be held "Low" for three cycles to guarantee that interrupt will be taken, although only one cycle is necessary to bring the processor out of SYNC.

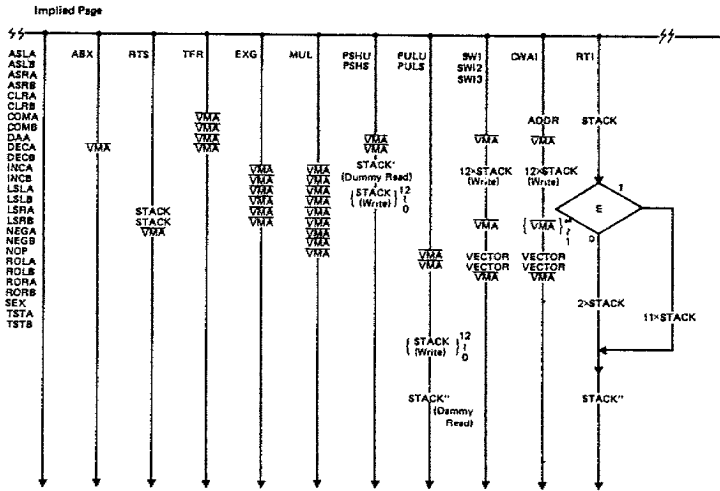
Figure 19 Sync Timing



(NOTE) Write operation during store instruction.

Figure 20 Address Bus Cycle-by-Cycle Performance





(NOTE) STACK': Address stored in stack pointer before execution.
 STACK'': Address set to stack pointer as the result of the execution.

Figure 20 Address Bus Cycle-by-Cycle Performance (Continued)

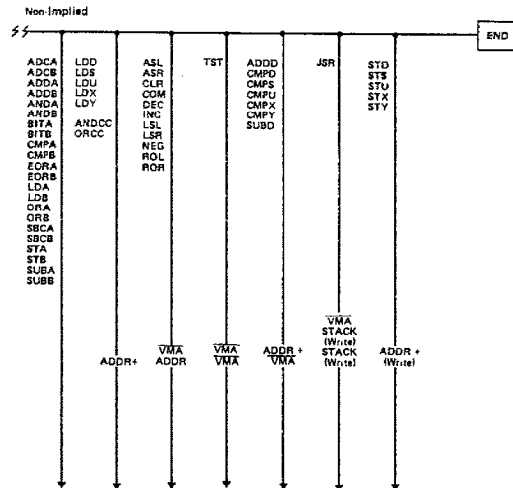


Figure 20 Address Bus Cycle-by-Cycle Performance (Continued)

Table 5 8-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADCA, ADCB	Add memory to accumulator with carry
ADDA, ADDB	Add memory to accumulator
ANDA, ANDB	And memory with accumulator
ASL, ASLA, ASLB	Arithmetic shift of accumulator or memory left
ASR, ASRA, ASRB	Arithmetic shift of accumulator or memory right
BITA, BITB	Bit test memory with accumulator
CLR, CLRA, CLRB	Clear accumulator or memory location
CMPA, CMPB	Compare memory from accumulator
COM, COMA, COMB	Complement accumulator or memory location
DAA	Decimal adjust A accumulator
DEC, DECA, DECB	Decrement accumulator or memory location
EORA, EORB	Exclusive or memory with accumulator
EXG R1, R2	Exchange R1 with R2 (R1, R2 = A, B, CC, DP)
INC, INCA, INCB	Increment accumulator or memory location
LDA, LDB	Load accumulator from memory
LSL, LSLA, LSLB	Logical shift left accumulator or memory location
LSR, LSRA, LSRB	Logical shift right accumulator or memory location
MUL	Unsigned multiply (A × B → D)
NEG, NEGA, NEGB	Negate accumulator or memory
ORA, ORB	Or memory with accumulator
ROL, ROLA, ROLB	Rotate accumulator or memory left
ROR, RORA, RORB	Rotate accumulator or memory right
SBCA, SBCB	Subtract memory from accumulator with borrow
STA, STB	Store accumulator to memory
SUBA, SUBB	Subtract memory from accumulator
TST, TSTA, TSTB	Test accumulator or memory location
TFR R1, R2	Transfer R1 to R2 (R1, R2 = A, B, CC, DP)

(NOTE) A, B, CC or DP may be pushed to (pulled from) either stack with PSHS, PSHU (PULS, PULU) instructions.

Table 6 16-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADDD	Add memory to D accumulator
CMPD	Compare memory from D accumulator
EXG D, R	Exchange D with X, Y, S, U or PC
LDD	Load D accumulator from memory
SEX	Sign Extend B accumulator into A accumulator
STD	Store D accumulator to memory
SUBD	Subtract memory from D accumulator
TFR D, R	Transfer D to X, Y, S, U or PC
TFR R, D	Transfer X, Y, S, U or PC to D

(NOTE) D may be pushed (pulled) to either stack with PSHS, PSHU (PULS, PULU) instructions.

Table 7 Index Register/Stack Pointer Instructions

Mnemonic(s)	Operation
CMPS, CMPU	Compare memory from stack pointer
CMPX, CMPY	Compare memory from index register
EXG R1, R2	Exchange D, X, Y, S, U or PC with D, X, Y, S, U or PC
LEAS, LEAU	Load effective address into stack pointer
LEAX, LEAY	Load effective address into index register
LDS, LDU	Load stack pointer from memory
LDX, LDY	Load index register from memory
PSHS	Push A, B, CC, DP, D, X, Y, U, or PC onto hardware stack
PSHU	Push A, B, CC, DP, D, X, Y, S, or PC onto user stack
PULS	Pull A, B, CC, DP, D, X, Y, U or PC from hardware stack
PULU	Pull A, B, CC, DP, D, X, Y, S or PC from user stack
STS, STU	Store stack pointer to memory
STX, STY	Store index register to memory
TFR R1, R2	Transfer D, X, Y, S, U or PC to D, X, Y, S, U or PC
ABX	Add B accumulator to X (unsigned)

Table 8 Branch Instructions

Mnemonic(s)	Operation
SIMPLE BRANCHES	
BEQ, LBEQ	Branch if equal
BNE, LBNE	Branch if not equal
BMI, LBMI	Branch if minus
BPL, LBPL	Branch if plus
BCS, LBCS	Branch if carry set
BCC, LBCC	Branch if carry clear
BVS, LBVS	Branch if overflow set
BVC, LBVC	Branch if overflow clear
SIGNED BRANCHES	
BGT, LBGT	Branch if greater (signed)
BGE, LBGE	Branch if greater than or equal (signed)
BEQ, LBEQ	Branch if equal
BLE, LBLE	Branch if less than or equal (signed)
BLT, LBLT	Branch if less than (signed)
UNSIGNED BRANCHES	
BHI, LBHI	Branch if higher (unsigned)
BHS, LBHS	Branch if higher or same (unsigned)
BEQ, LBEQ	Branch if equal
BLS, LBLS	Branch if lower or same (unsigned)
BLO, LBLO	Branch if lower (unsigned)
OTHER BRANCHES	
BSR, LBSR	Branch to subroutine
BRA, LBRA	Branch always
BRN, LBRN	Branch never

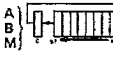
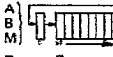
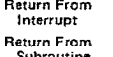
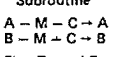
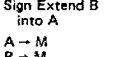
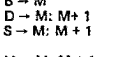
Table 9 Miscellaneous Instructions

Mnemonic(s)	Operation
ANDCC	AND condition code register
CWAI	AND condition code register, then wait for interrupt
NOP	No operation
ORCC	OR condition code register
JMP	Jump
JSR	Jump to subroutine
RTI	Return from interrupt
RTS	Return from subroutine
SWI, SWI2, SWI3	Software interrupt (absolute indirect)
SYNC	Synchronize with interrupt line

HD6809 ADDRESSING MODES

INSTRUCTION/ FORMS	ADDRESSING MODES												DESCRIPTION	5	3	2	1	0						
	IMPLIED			DIRECT			EXTENDED			IMMEDIATE									INDEXED ^①			RELATIVE		
	OP	~	#	OP	~	#	OP	~	#	OP	~	#							OP	~	#	OP	~	#
ABX	3A	3	1																B ← X ← X (UNSIGNED) A ← M ← C ← A B ← M ← C ← B	•	•	•	•	•
ADC ADCA ADCB				99 D9	4 4	2 2	B9 F9	5 5	3 3	89 C9	2 2	2 2	A9 E9	4+ 4+	2+ 2+									
ADD ADDA ADDB ADDD				9B DB D3	4 4 6	2 2 2	BB FB F3	5 5 7	3 3 3	8B CB C3	2 2 4	2 2 3	AB EB E3	4+ 4+ 6+	2+ 2+ 2+									
AND ANDA ANDB ANDCC				94 D4	4 4	2 2	B4 F4	5 5	3 3	84 C4 C	2 2 2	2 2 2	A4 E4 C	4+ 4+ 4+	2+ 2+ 2+									
ASL ASLA ASLB ASL	48 58	2 2	1 1																					
ASR ASRA ASRB ASR	47 57	2 2	1 1	08	6	2	78	7	3				68	6+	2+									
BCC LBCC				07	6	2	77	7	3				67	6+	2+									
BCS LBCS																24 10 24	3 5(6)	2 4	Branch C = 0 Long Branch C = 0	•	•	•	•	•
BEQ LBEQ																25 10 25	3 5(6)	2 4	Branch C = 1 Long Branch C = 1	•	•	•	•	•
BGE LBGE																27 10 27	3 5(6)	2 4	Branch Z = 1 Long Branch Z = 1	•	•	•	•	•
BGT LBGT																2C 10 2C	3 5(6)	2 4	Branch N ⊕ V = 0 Long Branch N ⊕ V = 0	•	•	•	•	•
BHI LBHI																2E 10 2E	3 5(6)	2 4	Branch ZV(N ⊕ V) = 0 Long Branch ZV(N ⊕ V) = 0	•	•	•	•	•
BHS LBHS																22 10 22	3 5(6)	2 4	Branch CVZ = 0 Long Branch CVZ = 0	•	•	•	•	•
BIT BITA BITB				95 D5	4 4	2 2	B5 F5	5 5	3 3	85 C5	2 2	2 2	A5 E5	4+ 4+	2+ 2+									
BLE LBLE																2F 10 2F	3 5(6)	2 4	Branch ZV(N ⊕ V) = 1 Long Branch ZV(N ⊕ V) = 1	•	•	•	•	•
BLO LBLO																25 10 25	3 5(6)	2 4	Branch C = 1 Long Branch C = 1	•	•	•	•	•
BLS LBLS																23 10 23	3 5(6)	2 4	Branch CVZ = 1 Long Branch CVZ = 1	•	•	•	•	•
BLT LBLT																2D 10 2D	3 5(6)	2 4	Branch N ⊕ V = 1 Long Branch N ⊕ V = 1	•	•	•	•	•
BMI LBMI																2B 10 2B	3 5(6)	2 4	Branch N = 1 Long Branch N = 1	•	•	•	•	•
BNE LBNE																26 10 26	3 5(6)	2 4	Branch Z = 0 Long Branch Z = 0	•	•	•	•	•
BPL LBPL																2A 10 2A	3 5(6)	2 4	Branch N = 0 Long Branch N = 0	•	•	•	•	•
BRA LBRA																20 16	3 5	2 3	Branch Always Long Branch/ Always	•	•	•	•	•
BRN LBRN																21 10 21	3 5	2 4	Branch Never Long Branch Never	•	•	•	•	•

(to be continued)

INSTRUCTION/ FORMS	HD6809 ADDRESSING MODES												DESCRIPTION	S	3	2	1	0						
	IMPLIED			DIRECT			EXTENDED			IMMEDIATE									INDEXED ^①			RELATIVE		
	OP	~	#	OP	~	#	OP	~	#	OP	~	#							OP	~	#	OP	~	#
OR ORA ORB ORCC				9A DA	4 4	2 2	8A FA	5 5	3 3	8A CA 1A	2 2 3	2 2 2	AA EA	4+ 4+	2+ 2+	A ∨ M → A B ∨ M → B CC ∨ IMM → CC	•	†	†	0	•			
PSH PSHS PSHU	34	5+ ^④	2													Push Registers on S Stack Push Registers on U Stack	•	•	•	•	•			
PUL PULS PULU	35 37	5+ ^④	2													Pull Registers from S Stack Pull Registers from U Stack	(-)	† ^③	(-)	† ^③	(-)			
ROL ROLA ROLB RQL	49 59	2 2	1 1	09	6	2	79	7	3				69	6+	2+	A)  B)  M) 	•	†	†	†	•			
ROR RORA RORB ROR	46 56	2 2	1 1	06	6	2	76	7	3				66	6+	2+	A)  B)  M) 	•	†	†	†	•			
RTI	3B	6/15	1													Return From Interrupt	(-)	† ^⑦	(-)	† ^⑦	(-)			
RTS	39	5	1													Return From Subroutine	•	•	•	•	•			
SBC SBCA SBCB				92 D2	4 4	2 2	B2 F2	5 5	3 3	82 C2	2 2	2 2	A2 E2	4+ 4+	2+ 2+	A - M - C → A B - M - C → B	† ^⑧	†	†	†	†			
SEX	1D	2	1													Sign Extend B into A	•	†	†	•	•			
ST STA STB STD STS				97 D7 DD 10	4 4 5 8	2 2 2 3	B7 F7 FD 10	5 5 6 7	3 3 3 4				A7 E7 ED 10	4+ 4+ 5+ 6+	2+ 2+ 2+ 3+	A → M B → M D → M: M + 1 S → M: M + 1	•	†	†	0	•			
STU STX STY				DF 9F 10 9F	5 5 8 8	2 2 3 3	FF BF 10 BF	6 6 7 4	3 3 4				EF AF 10 AF	5+ 5+ 6+ 3+	2+ 2+ 3+	U → M: M + 1 X → M: M + 1 Y → M: M + 1	•	†	†	0	•			
SUB SUBA SUBB SUBD				90 D0 93	4 4 6	2 2 2	B0 F0 B3	5 5 7	3 3 3	80 C0 83	2 2 4	2 2 3	A0 E0 A3	4+ 4+ 6+	2+ 2+ 2+	A - M → A B - M → B D - M: M + 1 → D	†	†	†	†	†			
SWI SWI1 ^⑩ SWI2 ^⑩ SWI3 ^⑩	3F 10 3F 11 3F	19 20	1 2													Software Interrupt1 Software Interrupt2 Software Interrupt3	•	•	•	•	•			
SYNC	13	≥2	1													Synchronize to Interrupt	•	•	•	•	•			
TFR R1, R2	1F	6	2													R1 → R2 [‡]	(-)	† ^⑨	(-)	† ^⑨	(-)			
TST TSTA TSTB TST	4D 5D	2 2	1 1	0D	6	2	7D	7	3				6D	6+	2+	Test A Test B Test M	•	†	†	0	•			

(NOTES)

- This column gives a base cycle and byte count. To obtain total count, and the values obtained from the INDEXED ADDRESSING MODES table.
- R1 and R2 may be any pair of 8 bit or any pair of 16 bit registers.
The 8 bit registers are: A, B, CC, DP
The 16 bit registers are: X, Y, U, S, D, PC
- EA is the effective address.
- The PSH and PUL instructions require 5 cycle plus 1 cycle for each byte pushed or pulled.
- 5(6) means: 5 cycles if branch not taken, 6 cycles if taken.
- SWI sets 1 and F bits. SWI2 and SWI3 do not affect I and F.
- Conditions Codes set as a direct result of the instruction.
- Value of half-carry flag is undefined.
- Special Case -- Carry set if b7 is SET.
- Condition Codes set as a direct result of the instruction if CC is specified, and not affected otherwise.

LEGEND:

OP	Operation Code (Hexadecimal)	Z	Zero (byte)
~	Number of MPU Cycles	V	Overflow, 2's complement
#	Number of Program Bytes	C	Carry from bit 7
+	Arithmetic Plus	†	Test and set if true, cleared otherwise
-	Arithmetic Minus	•	Not Affected
X	Multiply	CC	Condition Code Register
M	Complement of M	:	Concatenation
→	Transfer Into	∨	Logical or
H	Half-carry (from bit 3)	∧	Logical and
N	Negative (sign bit)	⊕	Logical Exclusive or

Table 11 Hexadecimal Values of Machine Codes

OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#	
00	NEG	Direct	6	2	30	LEAX	Indexed	4+	2+	80	NEG	Indexed	6+	2+	
01	*	↑			31	LEAY	↑	4+	2+	81	*	↑			
02	*				32	LEAS				4+	2+				
03	COM	↑	6	2	33	LEAU	↑	4+	2+	83	COM	↑	6+	2+	
04	LSR				34	PSHS				5+	2				64
05	*	↑			35	PULS	↑	5+	2	65	*	↑			
06	ROR				36	PSHU				5+	2				66
07	ASR	↑	6	2	37	PULU	↑	5+	2	67	ASR	↑	6+	2+	
08	ASL, LSL				38	*				68	ASL, LSL				6+
09	ROL	↑	6	2	39	RTS	↑	5	1	69	ROL	↑	6+	2+	
0A	DEC				3A	ABX				3	1				6A
0B	*	↑			3B	RTI	↑	6, 15	1	6B	*	↑			
0C	INC				3C	CWAI				20	2				6C
0D	TST	↑	6	2	3D	MUL	↑	11	1	6D	TST	↑	6+	2+	
0E	JMP				3E	*				6E	JMP				3+
0F	CLR	Direct	6	2	3F	SWI	Implied	19	1	6F	CLR	Indexed	6+	2+	
10	} See Next Page	—	—	—	40	NEGA	Implied	2	1	70	NEG	Extended	7	3	
11		—	—	—	41	*	↑			71	*	↑			
12	NOP	Implied	2	1	42	*				2	1				72
13	SYNC	Implied	2	1	43	COMA	↑	2	1			73	COM	↑	7
14	*	↑			44	LSRA				↑	2	1	74		
15	*				45	*	75	*							
16	LBRA	Relative	5	3	46	RORA	↑	2	1	76	ROR	↑	7	3	
17	LBSR	Relative	9	3	47	ASRA				2	1				77
18	*	↑			48	ASLA, LSLA	↑	2	1	78	ASL, LSL	↑	7	3	
19	DAA				Implied	2				1	49				ROLA
1A	ORCC	Immed	3	2	4A	DECA	↑	2	1	7A	DEC	↑	7	3	
1B	*	↑			4B	*				2	1				7B
1C	ANDCC				Immed	3	2	4C	INCA			↑	2	1	7C
1D	SEX	Implied	2	1	4D	TSTA	2	1	7D	TST	7				3
1E	EXG	↑	8	2	4E	*	↑	2	1	7E	JMP	↑	4	3	
1F	TFR				Implied	6				2	4F				CLRA
20	BRA	↑	3	2	50	NEGB	↑	2	1	80	SUBA	↑	2	2	
21	BRN				3	2				51	*				81
22	BHI	↑	3	2	52	*	↑	2	1	82	SBCA	↑	2	2	
23	BLS				3	2				53	COMB				2
24	BHS, BCC	↑	3	2	54	LSRB	↑	2	1	84	ANDA	↑	2	2	
25	BLO, BCS				55	*				85	BITA				2
26	BNE	↑	3	2	56	RORB	↑	2	1	86	LDA	↑	2	2	
27	BEQ				57	ASRB				2	1				87
28	BVC	↑	3	2	58	ASLB, LSLB	↑	2	1	88	EORA	↑	2	2	
29	BVS				59	ROLB				2	1				89
2A	BPL	↑	3	2	5A	DECB	↑	2	1	8A	ORA	↑	2	2	
2B	BMI				5B	*				8B	ADDA				2
2C	BGE	↑	3	2	5C	INCB	↑	2	1	8C	CMPX	↑	Immed	4	3
2D	BLT				5D	TSTB				2	1				
2E	BGT	↑	3	2	5E	*	↑	2	1	8E	LDX	↑	Immed	3	3
2F	BLE				Relative	3				2	5F				

LEGEND:
 ~ Number of MPU cycles (less possible push pull or indexed-mode cycles)
 # Number of program bytes
 * Denotes unused opcode

(to be continued)

OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#
90	SUBA	Direct	4	2	C6	LDB	Immed	2	2	FC	LDD	Extended	6	3
91	CMPA	↑	4	2	C7	*	↑			FD	STD	↑	6	3
92	SBCA	↑	4	2	C8	EORB	↑	2	2	FE	LDU	↓	6	3
93	SUBD	↑	6	2	C9	ADCB	↑	2	2	FF	STU	↓	6	3
94	ANDA	↑	4	2	CA	ORB	↑	2	2	2 Bytes Opcode				
95	BITA	↑	4	2	CB	ADDB	↑	2	2					
96	LDA	↑	4	2	CC	LDD	↑	3	3	1021	LBRN	Relative	5	4
97	STA	↑	4	2	CD	*	↑			1022	LBHI	↑	5(6)	4
98	EORA	↑	4	2	CE	LDU	↑	3	3	1023	LBLS	↑	5(6)	4
99	ADCA	↑	4	2	CF	*	↑			1024	LBHS, LBCC	↑	5(6)	4
9A	ORA	↑	4	2			↑			1025	LBCS, LBLO	↑	5(6)	4
9B	ADDA	↑	4	2	D0	SUBB	Direct	4	2	1026	LBNE	↑	5(6)	4
9C	CMPX	↑	6	2	D1	CMPB	↑	4	2	1027	LBEQ	↑	5(6)	4
9D	JSR	↑	7	2	D2	SBCB	↑	4	2	1028	LBVC	↑	5(6)	4
9E	LDX	↑	5	2	D3	ADDD	↑	6	2	1029	LBVS	↑	5(6)	4
9F	STX	Direct	5	2	D4	ANDB	↑	4	2	102A	LBPL	↑	5(6)	4
					D5	BITB	↑	4	2	102B	LBMI	↑	5(6)	4
A0	SUBA	Indexed	4+	2+	D6	LDB	↑	4	2	102C	LBGE	↑	5(6)	4
A1	CMPA	↑	4+	2+	D7	STB	↑	4	2	102D	LBLT	↑	5(6)	4
A2	SBCA	↑	4+	2+	D8	EORB	↑	4	2	102E	LBGT	↑	5(6)	4
A3	SUBD	↑	6+	2+	D9	ADCB	↑	4	2	102F	LBLE	Relative Implied	20	2
A4	ANDA	↑	4+	2+	DA	ORB	↑	4	2	103F	SWI2	Immed	5	4
A5	BITA	↑	4+	2+	DB	ADDB	↑	4	2	1083	CMPD	Immed	5	4
A6	LDA	↑	4+	2+	DC	LDD	↑	5	2	108C	CMPY	↑	5	4
A7	STA	↑	4+	2+	DD	STD	↑	5	2	108E	LDY	Immed	4	4
A8	EORA	↑	4+	2+	DE	LDU	↑	5	2	1093	CMPD	Direct	7	3
A9	ADCA	↑	4+	2+	DF	STU	Direct	5	2	109C	CMPY	↑	7	3
AA	ORA	↑	4+	2+			↑			109E	LDY	↑	6	3
AB	ADDA	↑	4+	2+	E0	SUBB	Indexed	4+	2+	109F	STY	Direct	6	3
AC	CMPX	↑	6+	2+	E1	CMPB	↑	4+	2+	10A3	CMPD	Indexed	7+	3+
AD	JSR	↑	7+	2+	E2	SBCB	↑	4+	2+	10AC	CMPY	↑	7+	3+
AE	LDX	↑	5+	2+	E3	ADDD	↑	6+	2+	10AE	LDY	↑	6+	3+
AF	STX	Indexed	5+	2+	E4	ANDB	↑	4+	2+	10AF	STY	Indexed	6+	3+
					E5	BITB	↑	4+	2+	10B3	CMPD	Extended	8	4
B0	SUBA	Extended	5	3	E6	LDB	↑	4+	2+	10BC	CMPY	↑	8	4
B1	CMPA	↑	5	3	E7	STB	↑	4+	2+	10BE	LDY	↑	7	4
B2	SBCA	↑	5	3	E8	EORB	↑	4+	2+	10BF	STY	Extended	7	4
B3	SUBD	↑	7	3	E9	ADCB	↑	4+	2+	10CE	LDS	Immed	4	4
B4	ANDA	↑	5	3	EA	ORB	↑	4+	2+	10DE	LDS	Direct	6	3
B5	BITA	↑	5	3	EB	ADDB	↑	4+	2+	10DF	STS	Direct	6	3
B6	LDA	↑	5	3	EC	LDD	↑	5+	2+	10EE	LDS	Indexed	6+	3+
B7	STA	↑	5	3	ED	STD	↑	5+	2+	10EF	STS	Indexed	6+	3+
B8	EORA	↑	5	3	EE	LDU	↑	5+	2+	10FE	LDS	Extended	7	4
B9	ADCA	↑	5	3	EF	STU	Indexed	5+	2+	10FF	STS	Extended	7	4
BA	ORA	↑	5	3			↑			113F	SWI3	Implied	20	2
BB	ADDA	↑	5	3	F0	SUBB	Extended	5	3	11B3	CMPU	Immed	5	4
BC	CMPX	↑	7	3	F1	CMPB	↑	5	3	11B8	CMPD	Immed	5	4
BD	JSR	↑	8	3	F2	SBCB	↑	5	3	1193	CMPU	Direct	7	3
BE	LDX	↑	6	3	F3	ADDD	↑	7	3	119C	CMPD	Direct	7	3
BF	STX	Extended	6	3	F4	ANDB	↑	5	3	11A3	CMPU	Indexed	7+	3+
					F5	BITB	↑	5	3	11AC	CMPD	Indexed	7+	3+
C0	SUBB	Immed	2	2	F6	LDB	↑	5	3	11B3	CMPU	Extended	8	4
C1	CMPB	↑	2	2	F7	STB	↑	5	3	11BC	CMPD	Extended	8	4
C2	SBCB	↑	2	2	F8	EORB	↑	5	3					
C3	ADDD	↑	4	3	F9	ADCB	↑	5	3					
C4	ADDB	↑	2	2	FA	ORB	↑	5	3					
C5	BITB	Immed	2	2	FB	ADDB	Extended	5	3					

(NOTE) All unused opcodes are not implemented and illegal

NOTE FOR USE

[1] Exceptional Operation of HD6809

(a) Exceptional Operations of DMA/BREQ, BA signals (#1)

HD6809 acknowledges the input signal level of DMA/BREQ at the end of each cycle, then determines whether the next sequence is MPU or DMA. When "Low" level is detected, HD6809 executes DMA

sequence by setting BA, BS to "High" level. However, in the conditions shown below the assertion of BA, BS delays one clock cycle.

< Conditions for the exception >

- (1) DMA/BREQ : "Low" for 6~13 cycles
- (2) DMA/BREQ : "High" for 3 cycles

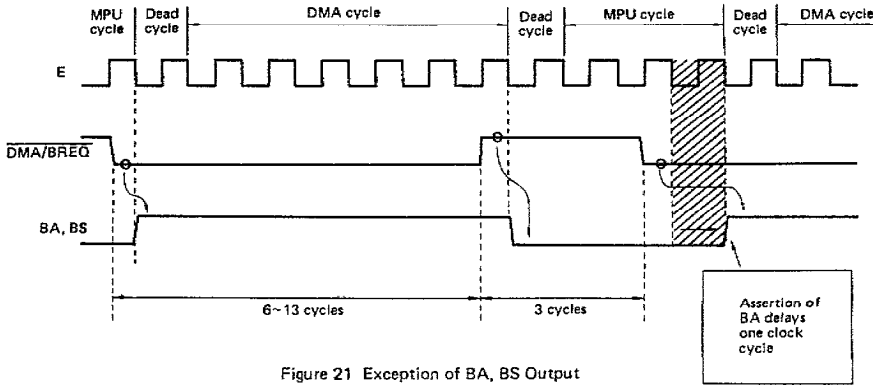


Figure 21 Exception of BA, BS Output

(b) Exceptional Operations of DMA/BREQ, BA signals (#2)

HD6809 includes a self refresh counter for the re-

verse cycle steal. And it is only cleared if DMA/BREQ is inactive ("High") for 3 or more MPU cycles. So 1 or 2 inactive cycle(s) doesn't affect the self refresh counter.

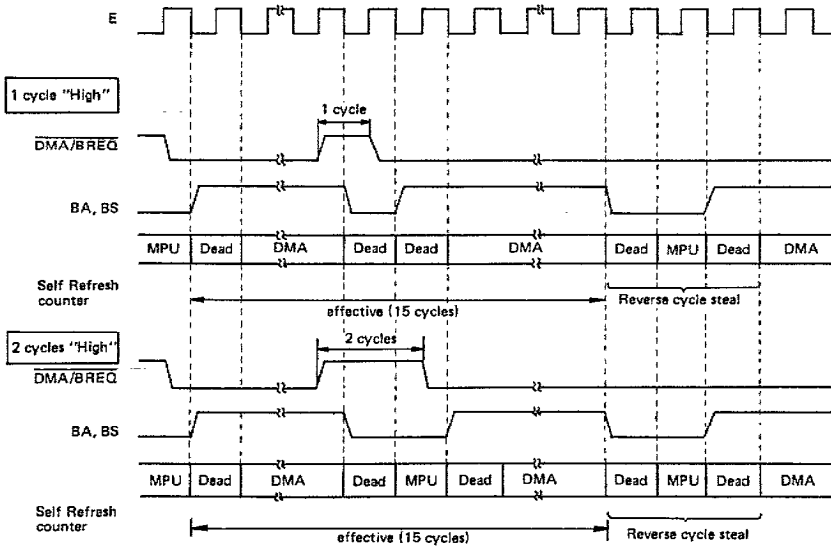


Figure 22 Exception of DMA/BREQ



- (c) **How to avoid these exceptional operations**
 It is necessary to provide 4 or more cycles for in- active $\overline{\text{DMA/BREQ}}$ level as shown in Fig. 23.

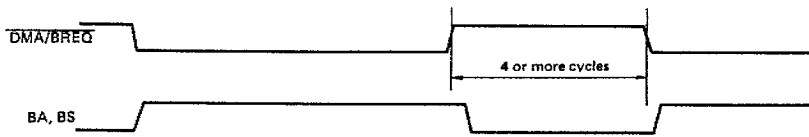


Figure 23 How to Avoid Exceptional Operations

[2] **Restriction for DMA Transfer**

There is a restriction for the DMA transfer in the HD6809 (MPU), HD6844 (DMAC) system. Please take care of following.

(a) **An Example of the System Configuration**

This restriction is applied to the following system.

- (1) $\overline{\text{DMA/BREQ}}$ is used for DMA request.
- (2) "Halt Burst Mode" is used for DMA transfer

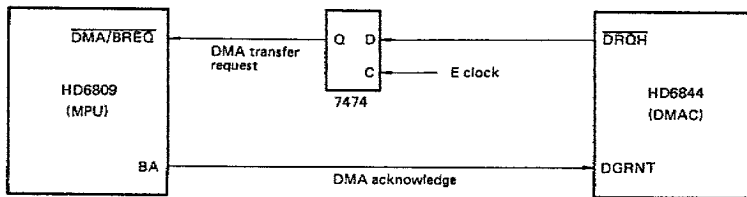


Figure 24 An Example of HD6809, HD6844 System

(The restriction is also applied to the system which doesn't use 7474 Flip-Flop. Fig. 24, Fig. 25 shows an example which uses 7474 for synchronizing DMA request with E.)

(b) **Restriction**

"The number of transfer Byte per one DMA Burst transfer must be less than or equal to 14."

Halt burst DMA transfer should be less than or equal to 14 cycles. In another word, the number stored into DMA Byte count register should be 0~14.

★ Please take care of the section [1](b) if 2 or more DMA channels are used for the DMA transfer.

reverse cycle steals once in 14 DMA cycles by taking back the bus control. In this case, however, the action taken by MPU is a little bit different from the DMAC.

As shown in Fig. 25, DMA controller can't stop DMA transfer (A) by BA falling edge and excutes an extra DMA cycle during HD6809 dead cycle. So MPU cycle is excuted right after DMA cycle, the Bus confliction occurs at the beginning of MPU cycle.

(c) **Incorrect operation of HD6809, HD6844 system**

"Incorrect Operation" will occur if the number of DMA transfer Byte is more than 14 bytes. If $\overline{\text{DMA/BREQ}}$ is kept in "Low" level HD6809 performs

(d) **How to impliment Halt Bust DMA transfer (> 14 cycles)**

Please use $\overline{\text{HALT}}$ input of HD6809 for the DMA request instead of $\overline{\text{DMA/BREQ}}$.

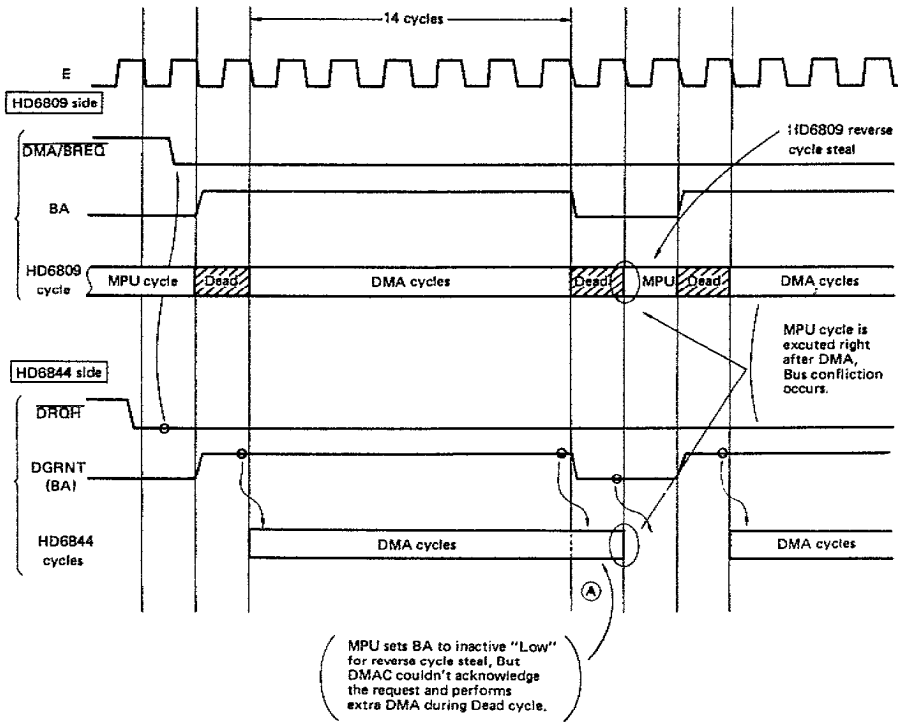


Figure 25 Comparison of HD6809, HD6844 DMA cycles

[3] Note for CLR Instruction

Cycle-by-cycle flow of CLR instruction (Direct, Extended, Indexed Addressing Mode) is shown below. In this sequence the content of the memory location specified by the operand is read before writing "00" into it. Note that status Flags, such as IRQ Flag, will be cleared by this extra data read operation when accessing the control/status register (sharing the same address between read and write) of peripheral devices.

Example: CLR (Extended)

Cycle #	Address	Data	R/W	Description
1	8000	7F	1	Opcode Fetch
2	8001	A0	1	Operand Address, High Byte
3	8002	00	1	Operand Address, Low Byte
4	FFFF	*	1	VMA Cycle
5	A000	80	1	Read the Data
6	FFFF	*	1	VMA Cycle
7	A000	00	0	Store Fixed "00" into Specified Location

* The data bus has the data at that particular address.

[4] Note for MRDY

HD6809 require synchronization of the MRDY input with the 4f clock. The synchronization necessitates an external oscillator as shown in Figure 26. The negative transition of the

MRDY signal, normally derived from the chip select decoding, must meet the t_{PCS} timing. MRDY's positive transition must occur with the rising edge of 4f.

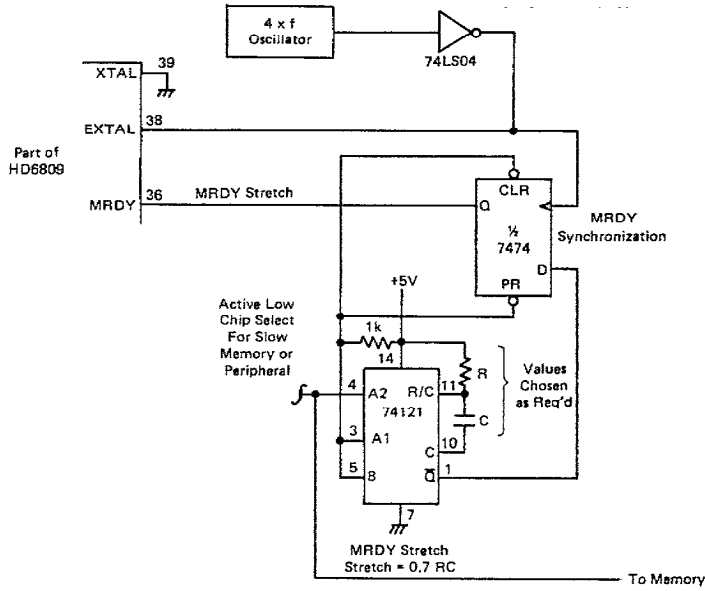


Figure 26 MRDY Synchronization

HD63B09, HD63C09

CMOS MPU (Micro Processing Unit)

Description

The HD6309 is the highest 8-bit micro-processor of HMCS6800 family, which is compatible with the conventional HD6809.

The HD6309 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

The HD6309 is complete CMOS device and its power dissipation is extremely low. Moreover, the SYNC and CWAI instruction makes low power application possible.

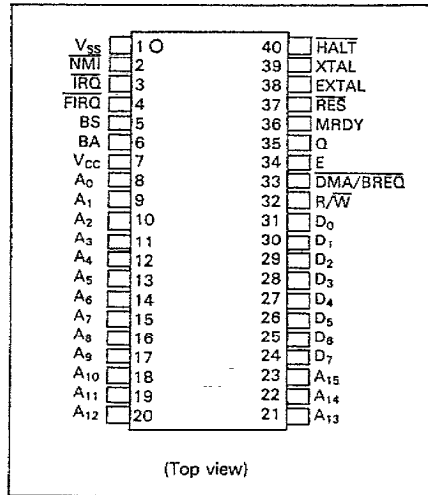
Features

- Hardware
 - Interfaces with all HMCS6800 peripherals
 - DMA transfer with no auto-refresh cycle
- Software: object code compatible with the HD6809
- Low power consumption mode (Sleep mode)
 - SYNC state of SYNC Instruction
 - WAIT state of CWAI Instruction
- On chip oscillator
- Wide operation range: $f=0.5$ to 3 MHz ($V_{CC}=5V \pm 10\%$)

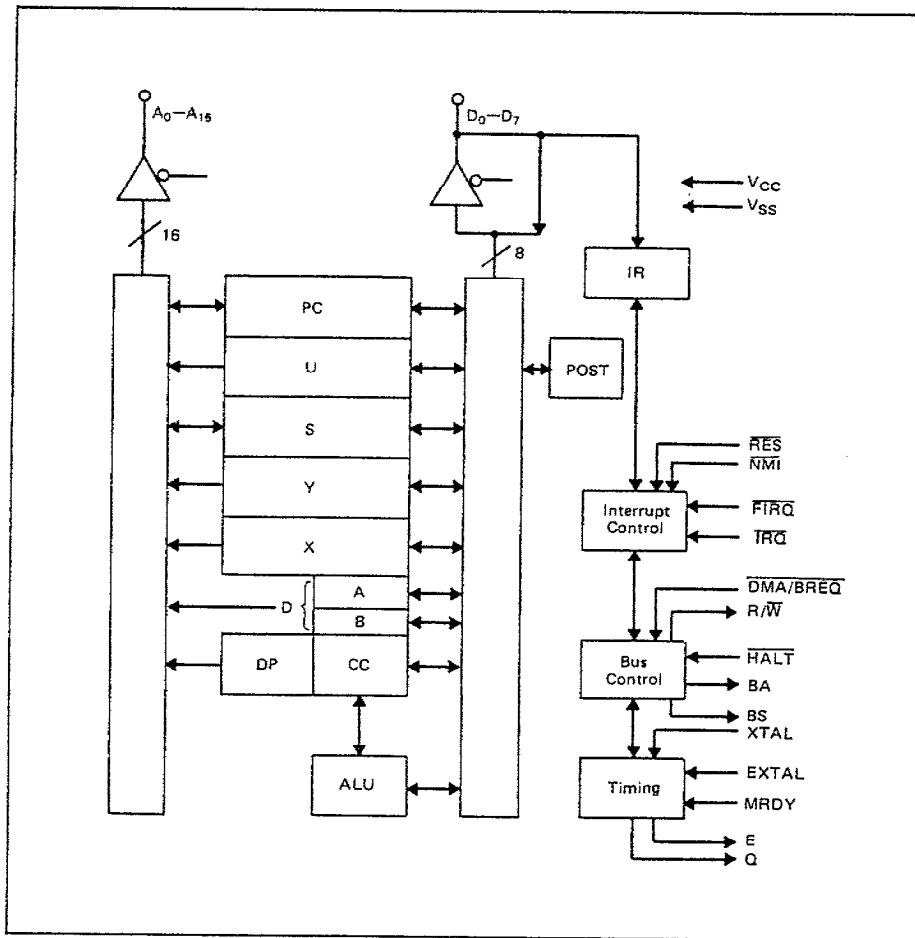
Type of Products

Type No.	Bus Timing
HD63B09P	2.0 MHz
HD63C09P	3.0 MHz

Pin Arrangement



Block Diagram



Programming Model

As shown in figure 1, the HD6309 adds three registers to the set available in the HD6800. The added registers are a direct page register, the user stack pointer and a second index register.

Accumulators (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D register. It is formed with the A register as the most significant byte.

Direct Page Register (DP)

The direct page register of the HD6309 serves to enhance the direct addressing mode. The contents of this register appears at the higher address outputs (A₈-A₁₅) during direct addressing instruction execution. This allows the direct mode to be used at any place in memory, under program control. To ensure HD6800 compatibility, all bits of this register are cleared during processor reset.

Index Registers (X, Y)

The index registers are used in indexed mode addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. In some indexed modes, the contents of the index register are incremented or decremented to point to the next item of tabular data. All four pointer registers (X, Y, U, S) may be used as index registers.

Stack Pointer (U, S)

The hardware stack pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the HD6309 point to the top of the stack, in contrast to the HD6800 stack pointer, which pointed to the next free location on the stack. The user stack pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. Both stack pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support push and pull instructions. This allows the HD6309 to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and

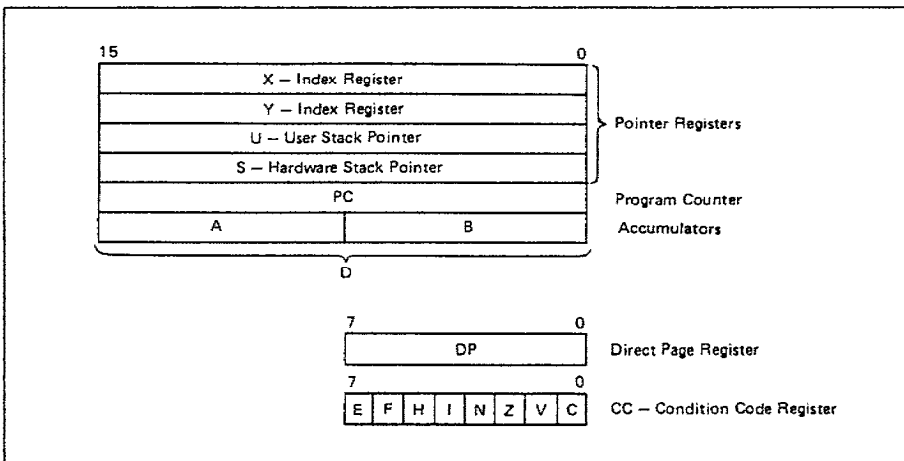


Figure 1. Programming Model of The Microprocessing Unit

modular programming.

Note: The stack pointers of the HD6309 point to the top of the stack, in contrast to the HD6800 stack pointer, which pointed to the next free location on stack.

Program Counter (PC)

The program counter is used by the processor to point to the address of the next instruction

to be executed by the processor. Relative addressing is provided allowing the program counter to be used like an index register in some situations.

Condition Code Register (CC)

The condition code register defines the state of the processor at any given time. See figure 2.

Condition Code Register Description

Bit 0 (C)

Bit 0 is the carry flag. It is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract-like instructions (CMP, NEG, SUB, SBC). Then, it is the complement of the carry from the binary ALU.

Bit 1 (V)

Bit 1 is the overflow flag. It is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB minus 1.

Bit 2 (Z)

Bit 2 is the zero flag. It is set to one if the result of the previous operation was identically zero.

Bit 3 (N)

Bit 3 is the negative flag. It contains exactly

the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to one.

Bit 4 (I)

Bit 4 is the $\overline{\text{IRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{IRQ}}$ line if this bit is set to one. NMI, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, RES, and SWI all set I to one; SWI2 and SWI3 do not affect I.

Bit 5 (H)

Bit 5 is the half-carry bit. It is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

Bit 6 (F)

Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the $\overline{\text{FIRQ}}$ line if

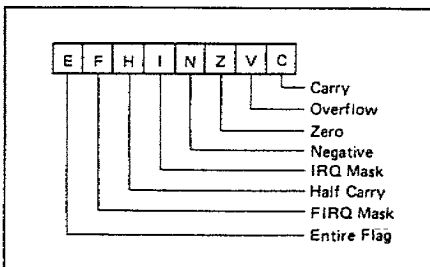


Figure 2. Condition Code Register Format

this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, SWI1 , and $\overline{\text{RES}}$ all set F to one. $\overline{\text{IRQ}}$, SWI2 and SWI3 do not affect F.

Bit 7 (E)

Bit 7 is the entire flag. Set to one, it indicates

that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the stacked CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the condition code register represents past action.

Signal Description

Power (V_{SS} , V_{CC})

Two pins supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is $+5.0 \text{ V} \pm 10\%$.

Address Bus ($A_0 - A_{15}$)

Sixteen pins output address information from the MPU onto the address bus. When the processor does not require the bus for a data transfer, it will output address FFFF_{16} , $\text{R}/\overline{\text{W}} =$

high, and $\text{BS} = \text{low}$. This is a "dummy access" or VMA cycle. All address bus drivers are made high impedance when the bus available output (BA) is high. Each pin will drive one Schottky TTL load or four LS TTL loads, and typically 90 pF.

Data Bus ($D_0 - D_7$)

These eight pins provide communication with the system bi-directional data bus. Each

Table 1. Pin Description

Symbol	Pin No.	I/O	Function
V_{SS}	1		Ground
$\overline{\text{NMI}}$	2	I	Non maskable interrupt
$\overline{\text{IRQ}}$	3	I	Interrupt request
$\overline{\text{FIRQ}}$	4	I	Fast interrupt request
BS, BA	5, 6	O	Bus status, Bus available
V_{CC}	7		+5 V power supply
$A_0 - A_{15}$	8-23	O	Address bus, bits 0-15
$D_7 - D_0$	24-31	I/O	Data bus, bits 0-7
$\text{R}/\overline{\text{W}}$	32	O	Read / Write output
$\overline{\text{DMA}}/\overline{\text{BREQ}}$	33	I	DMA Bus request
E, Q	34, 35	O	Clock signal
MRDY	36	I	Memory ready
$\overline{\text{RES}}$	37	I	Reset input
EXTAL, XTAL	38, 39	I	Oscillator connection
HALT	40	I	Halt input

pin will drive one Schottky TTL load or four LS TTL loads, and typically 130 pF.

Read/Write (R/W)

This signal indicates the direction of data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/W is made high impedance when BA is high. Refer to figures 27 and 28.

Reset ($\overline{\text{RES}}$)

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU, as shown in figure 3. During the reset operation internal transaction, the address bus outputs FFFF₁₆ to enter VMA state. The reset vectors are fetched from locations FFFE₁₆ and FFFF₁₆ (table 2) when interrupt acknowledge is true, ($\overline{\text{BA}} \cdot \overline{\text{BS}} = 1$). During initial power-on, the reset line should be held low until the clock oscillator is fully operational. See figure 4.

Because the HD6309 reset pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage ensures that all peripherals are out of the reset state before the processor.

Halt ($\overline{\text{HALT}}$)

A low level held on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When halted, the BA output is driven high indicating the buses are high impedance. BS is also high which

indicates the processor is in the halt or bus grant state (figure 5). While halted, the MPU will not respond to external interrupt requests ($\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$) although $\overline{\text{DMA/BREQ}}$ will always be accepted, and NMI or RES will be latched for later response. During the halt state, Q and E continue to run normally. Even if the MPU is running reset or is in the wait state for the CWAI and SYNC instructions, the MPU is placed in a halt state ($\overline{\text{BA}}$ and $\overline{\text{BS}} = \text{High}$) by pulling $\overline{\text{HALT}}$ to low.

Bus Available, Bus Status (BA, BS)

The BA output is an indication of an internal control signal which makes the MOS buses of the MPU high impedance. This signal does not imply that the bus will be available for more than one cycle. When BA goes low, an additional dead cycle will elapse before the MPU acquires the bus.

The BS output signal, when decoded with BA, represents the MPU state. See table 3.

Interrupt Acknowledge is indicated during both cycles of a hardware vector fetch ($\overline{\text{RES}}$, NMI, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, SWI, SWI2, SWI3). This signal, plus decoding of the lower four address lines, can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device. See table 2.

Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

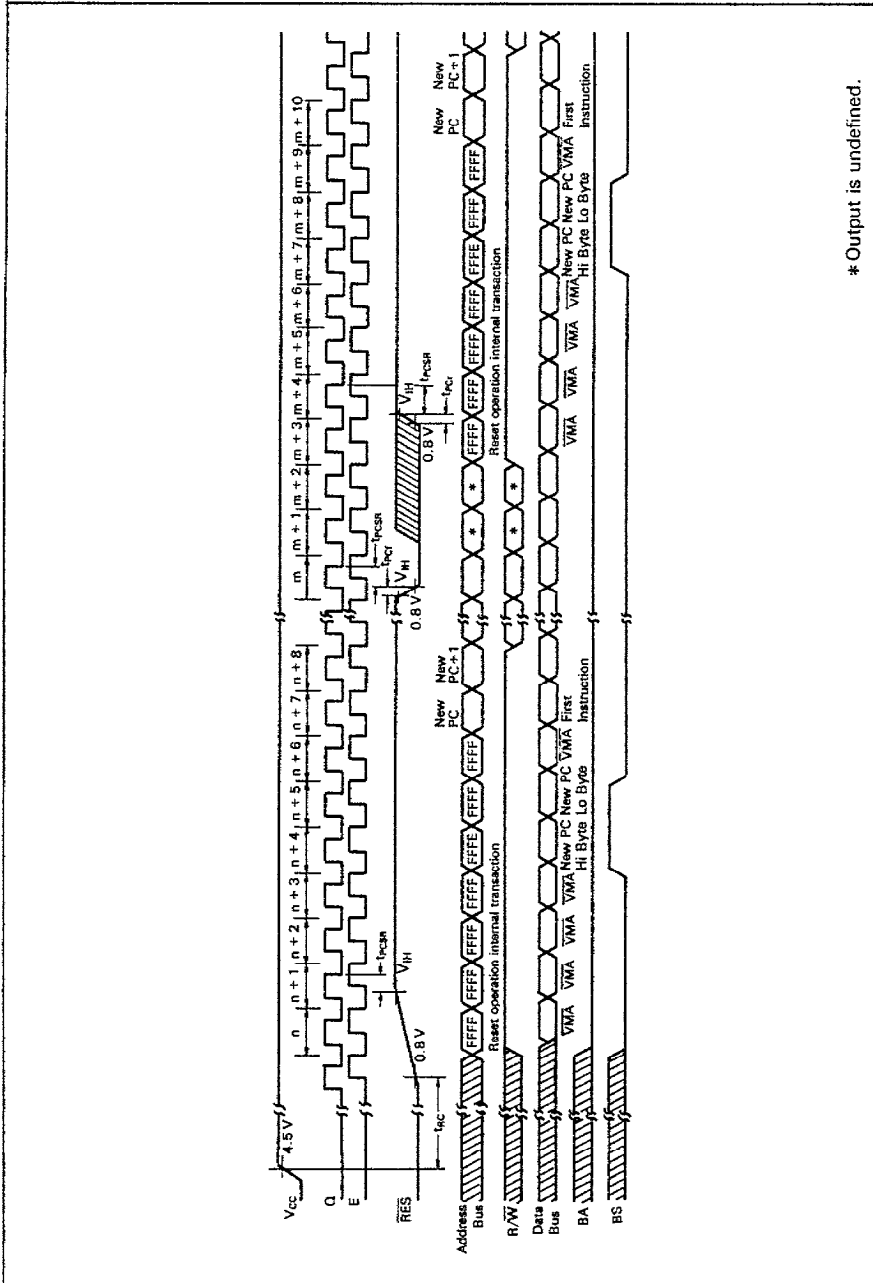
Halt/Bus Grant is true when the HD6309 is in a halt or bus grant condition.

Table 2. Memory Map for Interrupt Vectors

Memory Map for Vector Locations		Interrupt Vector Description
MS	LS	
FFFE	FFFF	$\overline{\text{RES}}$
FFFC	FFFD	NMI
FFFA	FFFB	SWI
FFF8	FFF9	$\overline{\text{IRQ}}$
FFF6	FFF7	$\overline{\text{FIRQ}}$
FFF4	FFF5	SWI2
FFF2	FFF3	SWI3
FFF0	FFF1	Reserved

Table 3. MPU State Definition

BA	BS	MPU State
0	0	Normal (Running)
0	1	Interrupt or RESET Acknowledge
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant



* Output is undefined.

Figure 3. \overline{RES} Timing

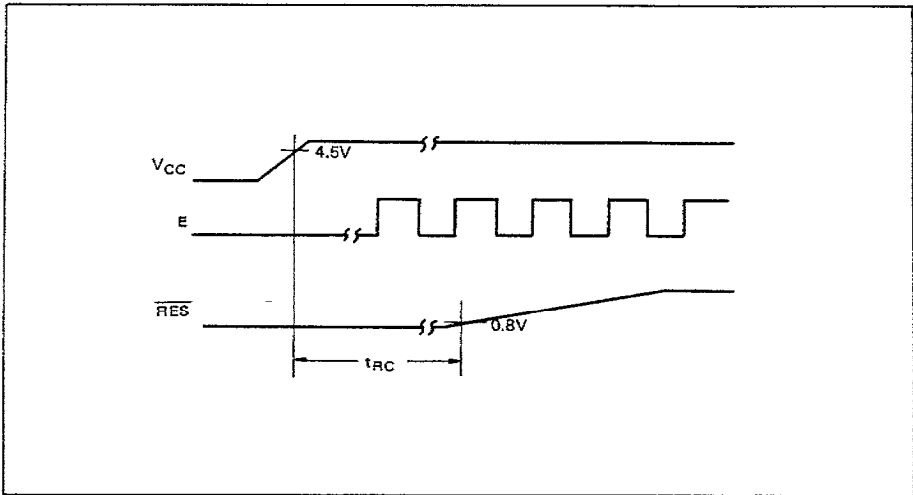


Figure 4. Crystal Connections and Oscillator Start Up

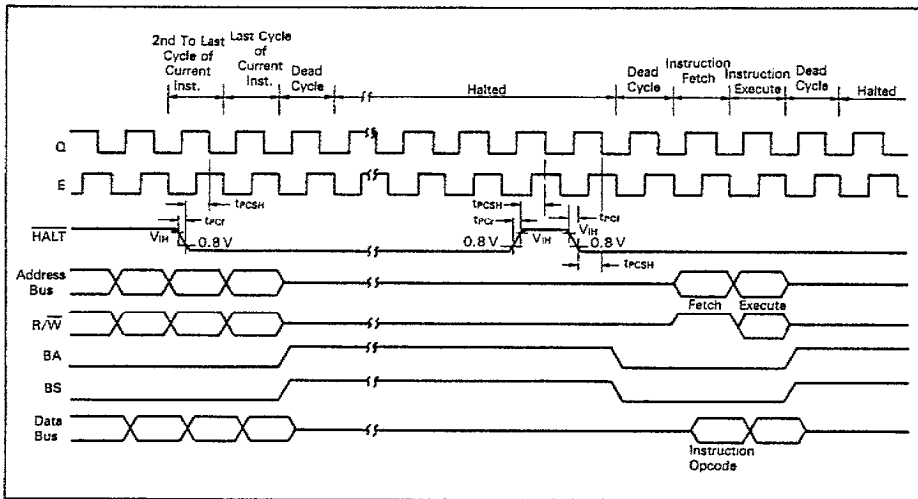


Figure 5. HALT and Single Instruction Execution for System Debug

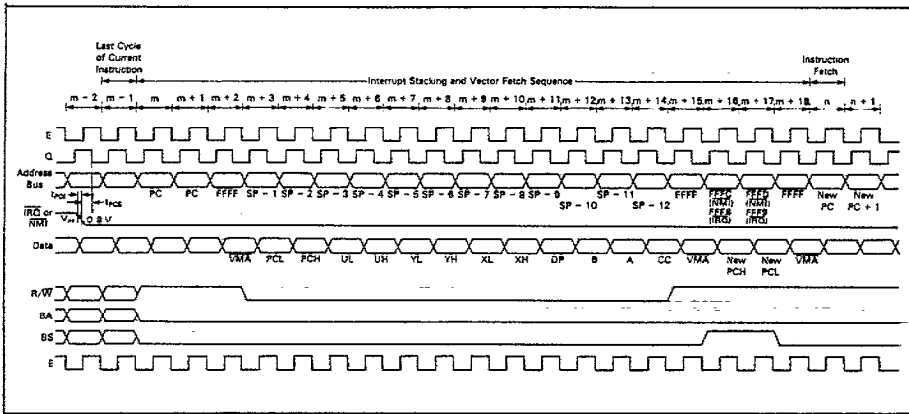


Figure 6. $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ Interrupt Timing

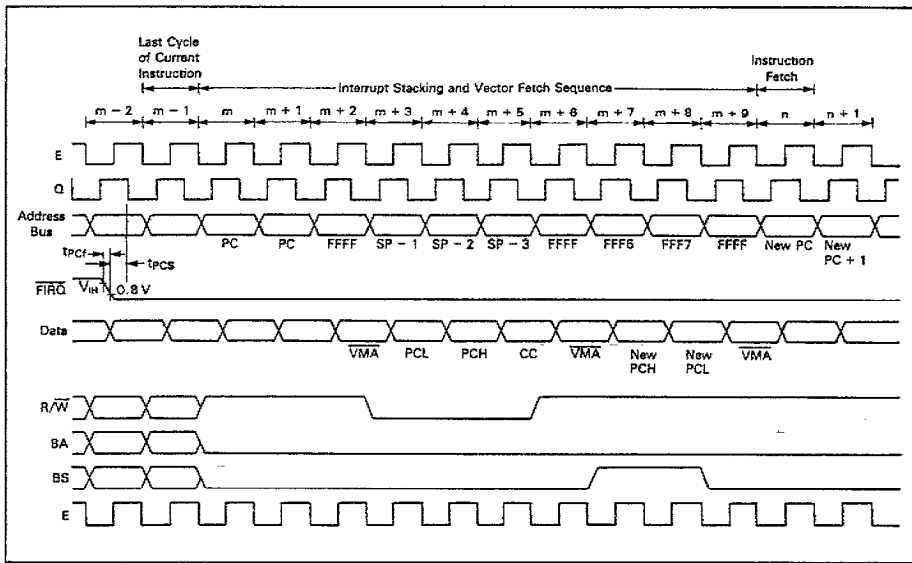


Figure 7. $\overline{\text{FIRQ}}$ Interrupt Timing

Non Maskable Interrupt ($\overline{\text{NMI}}$)

A negative edge on $\overline{\text{NMI}}$ requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program, and also has a higher priority than $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$ or software interrupts. During recognition of an $\overline{\text{NMI}}$, the entire machine state is saved on the hardware stack. After reset, an $\overline{\text{NMI}}$ will not be recognized until the first program load of the hardware stack pointer (S). The pulse width of $\overline{\text{NMI}}$ low must be at least one E cycle. If the $\overline{\text{NMI}}$ input does not meet the minimum set up (t_{PCS}) with respect to Q, the interrupt will not be recognized until the next cycle. See figure 6.

Fast Interrupt Request ($\overline{\text{FIRQ}}$)

A low level on $\overline{\text{FIRQ}}$ input will initiate a fast interrupt sequence provided its mask bit (F) in the CC is clear. This sequence has priority over the standard interrupt request ($\overline{\text{IRQ}}$). It is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See figure 7.

Interrupt Request ($\overline{\text{IRQ}}$)

A low level input on $\overline{\text{IRQ}}$ will initiate an interrupt request sequence provided the mask bit (I) in the CC is clear. Since $\overline{\text{IRQ}}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{\text{FIRQ}}$. $\overline{\text{IRQ}}$ also has a lower priority than $\overline{\text{FIRQ}}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See figure 6.

Note: $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, and $\overline{\text{IRQ}}$ requests are sampled on the falling edge of Q. One cycle is required for synchronization before these interrupts are recognized. The pending interrupt(s) will not be serviced until completion of the current instruction unless a SYNC or CWAI condition is present. If $\overline{\text{IRQ}}$ and $\overline{\text{FIRQ}}$ do not remain low until completion of the current instruction they may not be recognized. However, $\overline{\text{NMI}}$ is latched and need only remain low for one cycle.

XTAL, EXTAL

These two pins are connected with parallel resonant fundamental crystal, AT cut (figure 8). Alternately, the pin EXTAL may be used as an input for external timing with XTAL floating. The crystal or external frequency is four times the bus frequency. Proper RF layout techniques should be observed in the layout of printed circuit boards.

Note for Board Design of the Oscillation Circuit: In designing the board, the following notes should be taken when the crystal oscillator is used. See figure 9.

1. Crystal oscillator and load capacity C_{in} , C_{out} must be placed near the LSI as much as possible. (Normal oscillation may be disturbed when external noise is induced to pin 38 and 39.)
2. Pin 38 and 39 signal line should be wired apart from other signal line as much as possible. Don't wire them in parallel with other lines. (Normal oscillation may be disturbed when E or Q signal feeds back to pin 38 and 39.)

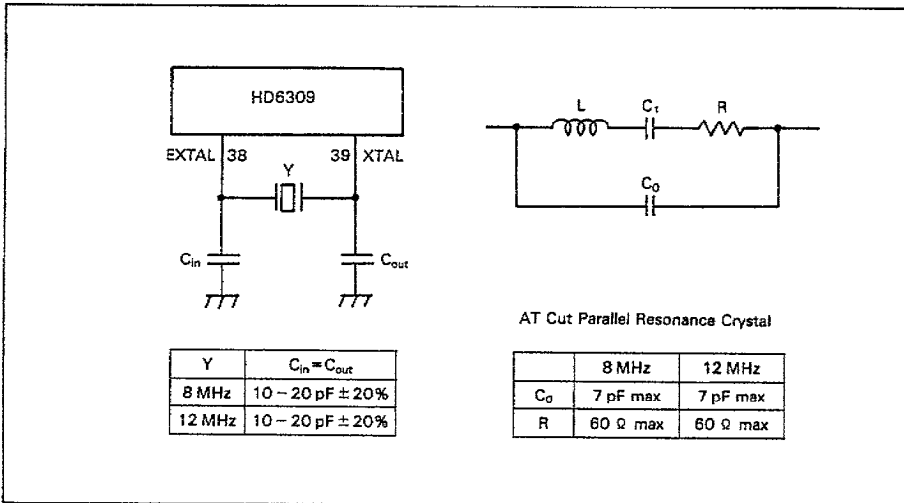


Figure 8. Crystal Connections

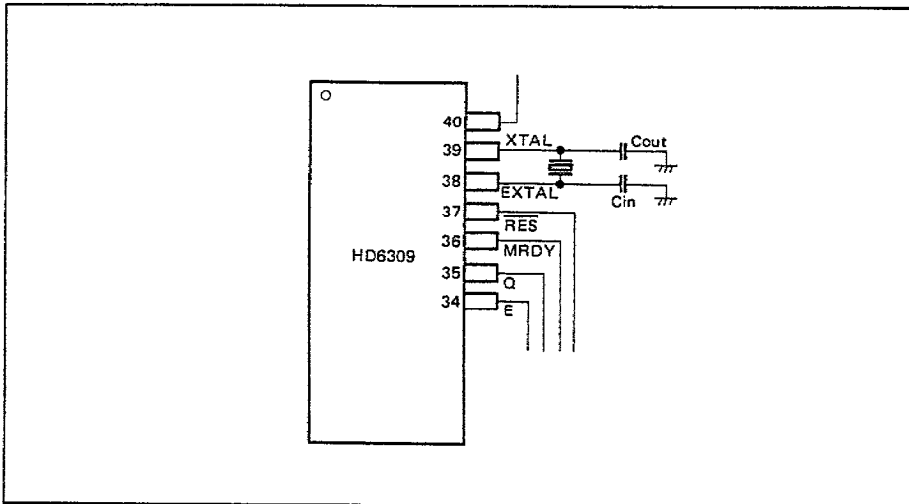


Figure 9. Board Design of the Oscillation Circuit

Designs to be Avoided: A signal line or a power source line must not cross or go near the oscillation circuit line as shown in figure 10 to prevent induction from these lines. The resistance between XTAL, EXTAL and other pins should be over 10 MΩ.

E, Q

E is similar to the HD6800 bus timing signal ϕ_2 . Q is a quadrature clock signal which leads E. Q has no parallel on the HD6800. Data is latched on the falling edge of E. Timing for E and Q is shown in figure 11.

Memory Ready (MRDY)

This input control signal allows stretching of E and Q to extend data-access time. E and Q operate normally while MRDY is high. When MRDY is low, E and Q may be stretched in integral multiples of half (1/2) bus cycles, thus allowing interface to slow memories, as shown in figure 12. MRDY may also be used to stretch clocks (for slow memory) when bus control has been transferred to an external device (through the use of HALT and DMA

$\overline{\text{BREQ}}$).

MRDY also stretches E and Q during dead cycles (see $\overline{\text{DMA/BREQ}}$, HALT). The maximum stretch is 5 microseconds.

During nonvalid memory access (No valid address on the address bus, with address bus = FFFF₁₆, R/W=high and BS=low, hereafter called VMA) MRDY has no effect on stretching E and Q: this inhibits slowing the processor during "don't care" bus accesses. During the reset operation internal transaction (see figure 3) as well, VMA is entered to prevent E and Q stretching.

DMA Bus Request ($\overline{\text{DMA/BREQ}}$)

The $\overline{\text{DMA/BREQ}}$ input provides a method of suspending execution and acquiring the MPU bus for another use, as shown in figure 13. Typical uses include DMA and dynamic memory refresh.

A low level on this pin will stop instruction execution at the end of the current cycle to release the bus. $\overline{\text{DMA/BREQ}}$ input must be

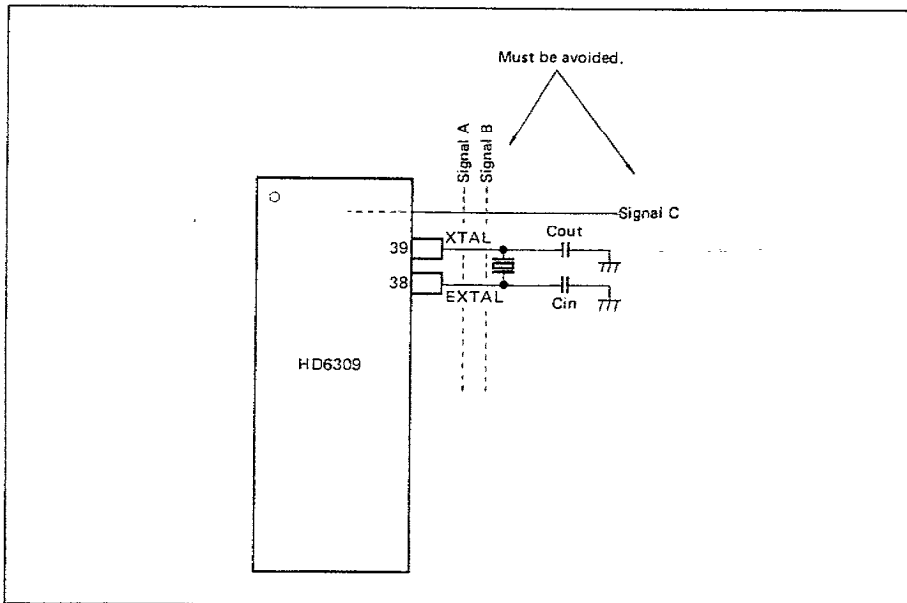


Figure 10. Example of Normal Oscillation Disturbed

stable before set up time t_{pcsd} , synchronized with E and Q; DMA BREQ logic levels must be switched while Q is high (figure 13). The MPU will acknowledge DMA BREQ by setting BA and BS high. DMA cycle is continued by holding DMA BREQ low (figure 14). The HD6309 does not perform the auto-refresh executed in the HD6809.

Typically, the DMA controller will request to use the bus by asserting DMA/BREQ pin low on the leading edge of E. When the MPU replies by setting BA and BS to one, that cycle will be a dead cycle used to transfer bus mastership to the DMA controller.

False memory accesses may be prevented during dead cycles by developing a system DMAVMA signal which is low in any cycle

when BA has changed.

When BA goes low (a result of $\overline{\text{DMA BREQ}} = \text{high}$), another dead cycle will elapse before the MPU accesses memory, to allow transfer of bus mastership without contention.

During a DMA cycle (also during dead cycle), external interrupt requests $\overline{\text{IRQ}}$ and $\overline{\text{FIRQ}}$ are not accepted. However, an interrupt on $\overline{\text{NMI}}$ having an internal latch can be executed on completion of the current instruction execution by releasing $\overline{\text{DMA BREQ}}$.

The $\overline{\text{DMA BREQ}}$ input should be tied high during the reset operation internal transaction (in VMA state in which the address bus outputs FFFF_{16}). See figure 21.

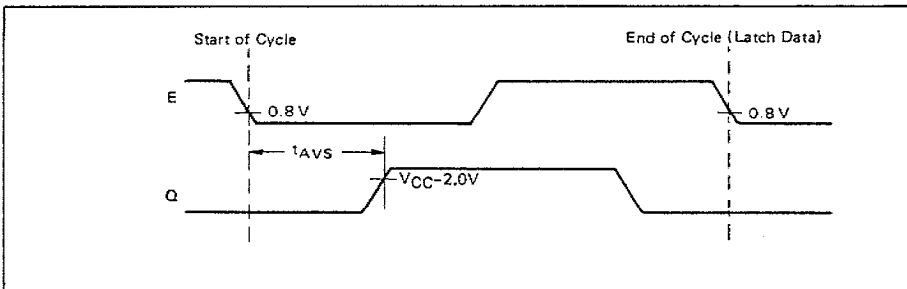


Figure 11. E/Q Relationship

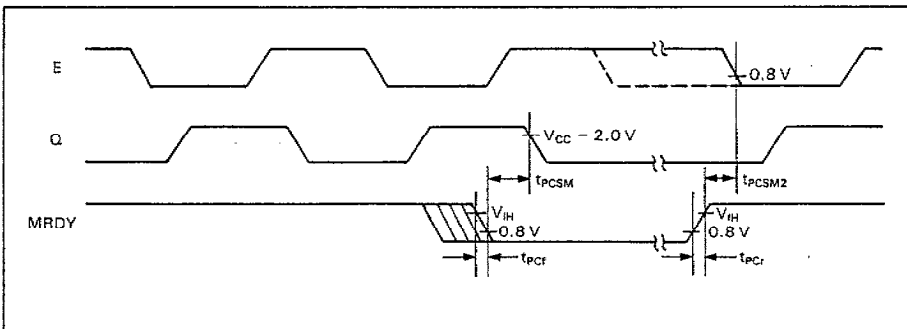


Figure 12. MRDY Clock Stretching

MPU Operation

During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This sequence begins at RES and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter

normal MPU operation are: SWI, SWI2, SWI3, CWAI, RTI and SYNC. An interrupt, HALT or DMA/BREQ can also alter the normal execution of instructions. Figure 15 illustrates the flow chart for the HD6309.

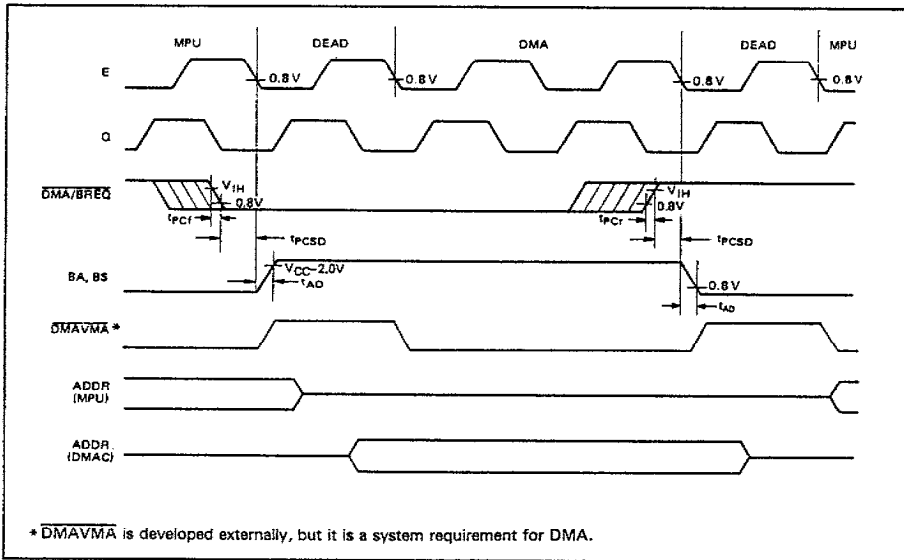


Figure 13. Typical DMA Timing

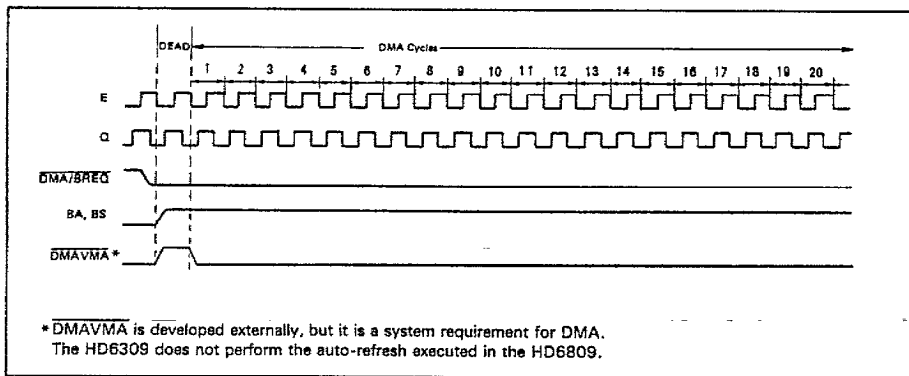
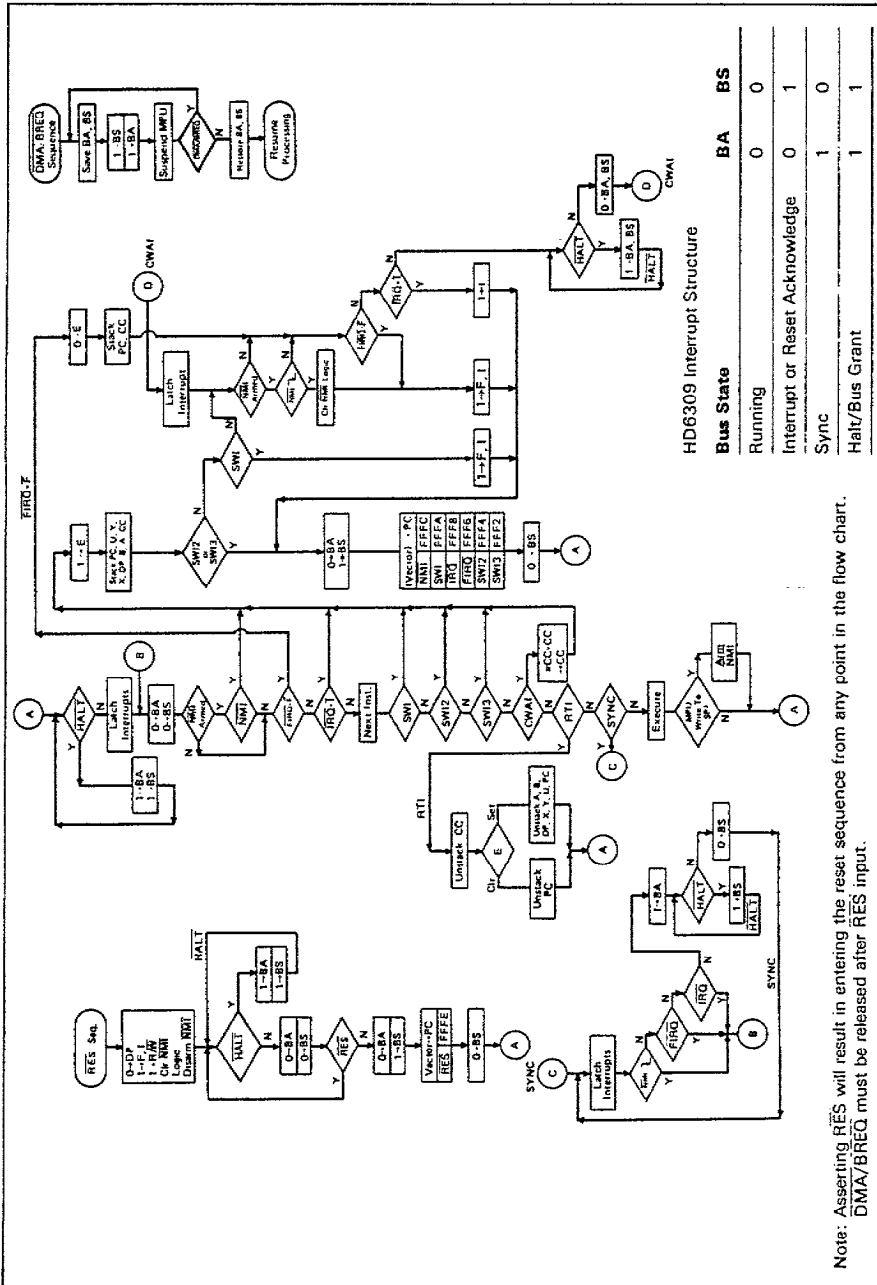


Figure 14. DMA Timing



Note: Asserting RES will result in entering the reset sequence from any point in the flow chart. DMA/BREQ must be released after RES input.

Figure 15. Flowchart for HD6309 Instruction

Addressing Modes

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The HD6309 has the most complete set of addressing modes available on any microcomputer today. For example, the HD6309 has 59 basic instructions, however, it recognizes 1464 different variations of instructions and addressing modes. The addressing modes support modern programming techniques. The following addressing modes are available on the HD6309:

- Implied (includes accumulator)
- Immediate
- Extended
- Extended indirect
- Direct
- Register
- Indexed
 - Zero-offset
 - Constant offset
 - Accumulator offset
 - Auto increment, decrement
- Indexed indirect
- Relative
- Program counter relative

Implied (Includes Accumulator)

In this addressing mode, the opcode of the instruction contains all the address information necessary. Examples of implied addressing are: ABX, DAA, SWI, ASRA, and CLR.B.

Immediate Addressing

In immediate addressing, the effective address of the data is the location immediately following the opcode (i.e., the data to be used in the instruction immediately follows the opcode of the instruction). The HD6309 uses both 8- and 16-bit immediate values depending on the size of the argument specified by the opcode. Examples of instructions with immediate addressing are:

```
LDA =$20
LDX =$F000
LDY =CAT
```

Note: \$ signifies immediate addressing, \$ signifies hexadecimal value.

Extended Addressing

In extended addressing, the contents of the two bytes immediately following the opcode fully specify the 16-bit effective address used by the instruction. Note that the address

generated by an extended instruction defines an absolute address and is not position independent. Examples of extended addressing include:

```
LDA CAT
STX MOUSE
LDD $2000
```

Extended Indirect

As a special case of indexed addressing (discussed below), one level of indirection may be added to extended addressing. In extended indirect, the two bytes following the postbyte of an indexed instruction contain the address of the data.

```
LDA [CAT]
LDX [$FFFE]
STU [DOG]
```

Direct Addressing

Direct addressing is similar to extended addressing except that only one byte of address follows the opcode. This byte specifies the lower 8 bits of the address to be used. The upper 8 bits of the address are supplied by the direct page register. Since only one byte of address is required in direct addressing, this mode requires less memory and executes faster than extended addressing. Of course, only 256 locations (one page) can be accessed without redefining the contents of the DP register. Since the DP register is set to \$00 on reset, direct addressing on the HD6309 is compatible with direct addressing on the HD6800. Indirection is not allowed in direct addressing. Some examples of direct addressing are:

```
LDA $30
SETDP $10 (Assembler directive)
LDB $1030
LDD <CAT
```

Note: < is an assembler directive which forces direct addressing.

Register Addressing

Some opcodes are followed by a byte that defines a register or set of registers to be used by the instruction. This is called a postbyte. Some examples of register addressing are:

```
TFR X,Y Transfers X into Y
EXG A,B Exchanges A with B
PSHS A, B, X, Y Push Y, X, B, and A onto S
```


PULU X, Y, D Pull D, X, and Y from U

Indexed Addressing

In all indexed addressing, one of the pointer registers (X, Y, U, S, and sometimes PC) is used in a calculation of the effective address of the operand to be used by the instruction. Five basic types of indexing are available and are discussed below. The postbyte of an indexed instruction specifies the basic type and

variation of the addressing mode as well as the pointer register to be used. Figure 16 lists the legal formats for the postbyte. Table 4 gives the assembler form and the number of cycles and bytes added to the basic values for indexed addressing for each variation.

Zero-Offset Indexed: In this mode, the selected pointer register contains the effective address of the data to be used by the instruction. This is the fastest indexing mode.

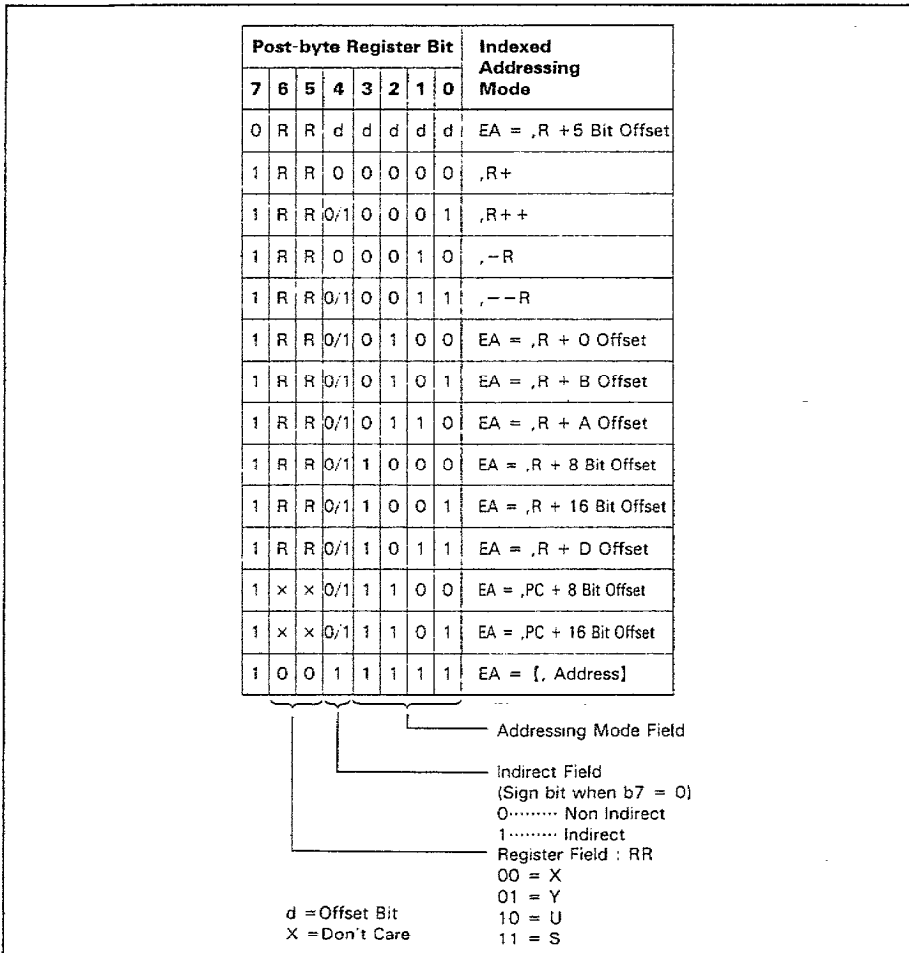


Figure 16. Indexed Addressing Postbyte Register Bit Assignments

Examples are:
 LDD 0, X
 LDA S

5-bit (-16 to +15)
 8-bit (-128 to +127)
 16-bit (-32768 to +32767)

Constant Offset Indexed: In this mode, a two's-complement offset and the contents of one of the pointer registers are added to form the effective address of the operand. The pointer register's initial content is unchanged by the addition.

The two's complement 5-bit offset is included in the postbyte and, therefore, is most efficient in use of bytes and cycles. The two's complement 8-bit offset is contained in a single byte following the postbyte. The two's complement 16-bit offset is in the two bytes following the postbyte. In most cases the programmer need not be concerned with the size of this offset since the assembler will select the optimal size automatically.

Three sizes of offsets are available:

Table 4. Indexed Addressing Mode

Type	Forms	Non Indirect		Indirect	
		Assembler Form	Postbyte OP Code	++ ~ # Assembler Form	Postbyte OP Code ++ ~ #
Constant Offset From R (2's Complement Offsets)	No Offset	,R	1RR00100 0 0	[,R]	1RR10100 3 0
	5 Bit Offset	n,R	ORRnnnnn 1 0	defaults to 8-bit	
	8 Bit Offset	n,R	1RR01000 1 1	[n, R]	1RR11000 4 1
	16 Bit Offset	n,R	1RR01001 4 2	[n, R]	1RR11001 7 2
Accumulator Offset From R (2's Complement Offsets)	A Register Offset	A,R	1RR00110 1 0	[A, R]	1RR10110 4 0
	B Register Offset	B,R	1RR00101 1 0	[B, R]	1RR10101 4 0
	D Register Offset	D,R	1RR01011 4 0	[D, R]	1RR11011 7 0
Auto Increment/Decrement R	Increment By 1	,R+	1RR00000 2 0	not allowed	
	Increment By 2	,R++	1RR00001 3 0	[,R ++]	1RR10001 6 0
	Decrement By 1	,-R	1RR00010 2 0	not allowed	
	Decrement By 2	,--R	1RR00011 3 0	[,--R]	1RR10011 6 0
Constant Offset From PC (2's Complement Offsets)	8 Bit Offset	n, PCR	1xx01100 1 1	[n, PCR]	1xx11100 4 1
	16 Bit Offset	n, PCR	1xx01101 5 2	[n, PCR]	1xx11101 8 2
Extended Indirect	16 Bit Address			[n]	10011111 5 2

R = X, Y, U or S
 x = Don't Care
 RR:
 00=X
 01=Y
 10=U
 11=S

~ and † indicate the number of additional cycles and bytes for the particular variation.

Examples of constant-offset indexing are:

```
LDA    23, X
LDX    -2, S
LDY    300, X
LDU    CAT, Y
```

Accumulator Offset Indexed: This mode is similar to constant offset indexed except that the two's-complement value in one of the accumulators (A, B or D) and the contents of one of the pointer registers are added to form the effective address of the operand. The contents of both the accumulator and the pointer register are unchanged by the addition. The postbyte specifies which accumulator to use as an offset and no additional bytes are required. The advantage of an accumulator offset is that the value of the offset can be calculated by a program at run-time.

Some examples are:

```
LDA    B, Y
LDX    D, Y
LEAX   B, X
```

Auto Increment/Decrement Indexed: In the auto increment addressing mode, the pointer register contains the address of the operand. Then, after the pointer register is used it is incremented by one or two. This addressing mode is useful in stepping through tables, moving data, or for the creation of software stacks. In auto decrement, the pointer register is decremented prior to use as the address of the data. The use of auto decrement is similar to that of auto increment; but the tables, etc, are scanned from high to low addresses. The size of the increment/decrement can be either one or two to allow for tables of either 8-or 16-bit data to be accessed, selectable by the programmer. The pre-decrement, post-increment nature of these modes allow them to be used to create additional software stacks that behave identically to the U and S stacks.

Some examples of the auto increment/decrement addressing modes are:

```
LDA    .X+
STD    .Y++
LDB    .-Y
LDX    .--S
```

Care should be taken in performing operations on 16-bit pointer registers (X, Y, U, S) where the same register is used to calculate the effective address.

Consider the following instruction:

```
STX 0, X++ (X initialized to 0)
```

The desired result is to store a 0 in locations \$0000 and \$0001 then increment X to point to \$0002. In reality, the following occurs:

```
0→temp    calculate the EA; temp is a
            holding register
X+2→X     perform autoincrement
X→(temp)  do store operation
```

Indexed Indirect

All of the indexing modes with the exception of auto increment/decrement by one, or a ± 4 -bit offset may have an additional level of indirection specified. In indirect addressing, the effective address is contained at the location specified by the contents of the index register plus any offset. In the example below, the A accumulator is loaded indirectly using an effective address calculated from the index register and an offset.

Before Execution:

```
A = X X (don't care)
X = $F000
```

```
$0100    LDA[$10, X]    EA is now $F010
$F010    $F1            $F150 is now the
$F011    $50           new EA
$F150    $AA
```

After Execution:

```
A = $AA (Actual Data Loaded)
X = $F000
```

All modes of indexed indirect are included except those which are meaningless (e.g., auto increment/decrement by 1 indirect). Some examples of indexed indirect are:

```
LDA    [X]
LDD    [10,S]
LDA    [B,Y]
LDD    [X++]
```

Relative Addressing

The byte(s) following the branch opcode is (are) treated as a signed offset which may be added to the program counter. If the branch condition is true then the calculated address (PC + signed offset) is loaded into the program counter. Program execution continues at the new location as indicated by the PC.

Short (1 byte offset) and long (2 bytes offset) relative addressing modes are available. All of memory can be reached in long relative addressing as an effective address is interpreted modulo 2^{16} . Some examples of relative addressing are:

	BEQ	CAT	(short)
	BGT	DOG	(short)
CAT	LBEQ	RAT	(long)
DOG	LBGT	RABBIT	(long)
	.		
	.		
RAT	NOP		
RABBIT	NOP		

Program Counter Relative

The PC can be used as the pointer register with 8-or 16-bit signed offsets. As in relative

addressing, the offset is added to the current PC to create the effective address. The effective address is then used as the address of the operand or data. Program counter relative addressing is used for writing position independent programs. Tables related to a particular routine will maintain the same relationship after the routine is moved, if referenced relative to the program counter. Examples are:

```
LDA    CAT, PCR
LEAX   TABLE, PCR
```

Since program counter relative is a type of indexing, an additional level of indirection is available.

```
LDA    [CAT, PCR]
LDU    [DOG, PCR]
```

HD6309 Instruction Set

The instruction set of the HD6309 is similar to that of the HD6800 and is upward compatible at the source code level. The number of opcodes has been reduced from 72 to 59, but because of the expanded architecture and additional addressing modes, the number of available opcodes (with different addressing modes) has risen from 197 to 1464.

Some of the instructions and addressing modes are described in detail below:

PSHU/PSHS

The push instructions can push onto either the hardware stack (S) or user stack (U) any single register, or set of registers with a single instruction.

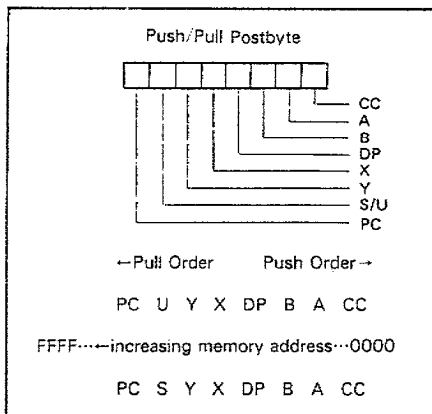


Figure 17. Push and Pull Order

PULU/PULS

The pull instructions have the same capability of the push instruction, in reverse order. The byte immediately following the push or pull opcode determines which register or registers are to be pushed or pulled. The actual PUSH/PULL sequence is fixed: each bit defines a unique register to push or pull, as shown in figure 17.

TFR/EXG

Within the HD6309, any register may be transferred to or exchanged with another of like-size: i.e., 8-bit to 8-bit or 16-bit to 16-bit. Bits 4-7 of the postbyte define the source register, while bits 0-3 represent the destination register (figure 18). They are denoted as follows:

0000-D	0101-PC
0001-X	1000-A
0010-Y	1001-B
0011-U	1010-CC
0100-S	1011-DP

Note: All other combinations are undefined and invalid.

LEAX/LEAY/LEAU/LEAS

The LEA (load effective address) works by calculating the effective address used in an indexed instruction and stores that address value, rather than the data at that address, in a pointer register. This makes all the features of the internal addressing hardware available to the programmer. Some of the implications of this instruction are illustrated in table 5.

The LEA instruction also allows the user to access data in a position independent manner. For example:

```
LEAX MSG1, PCR
LBSR PDATA(Print message
          routine)
```

```
MSG1 FCC 'MESSAGE'
```

This sample program prints: 'MESSAGE'. By writing MSG1, PCR, the assembler computes the distance between the present address and MSG1. This result is placed as a constant into the LEAX instruction which will be indexed from the PC value at the time of execution. No matter where the code is located, when it is executed, the computed offset from the PC will put the absolute address of MSG1 into the X pointer register. This code is totally position independent.

The LEA instructions are very powerful and use an internal holding register (temp). Care must be exercised when using the LEA instructions with the autoincrement and autodecrement addressing modes due to the sequence of internal operations. The LEA internal sequence is outlined as follows:

- LEAa ,b+ (any of the 16-bit pointer registers X, Y, U, or S may be substituted for a and b)
- 1. b→temp (calculate the EA)
- 2. b + 1→b (modify b, postincrement)
- 3. temp→a (load a)

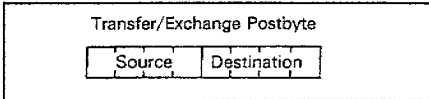


Figure 18. TFR/EXG Format

Table 5. LEA Examples

Instruction	Operation	Comment
LEAX 10, X	X+10→X	Adds 5-bit constant 10 to X
LEAX 500, X	X+500→X	Adds 16-bit constant 500 to X
LEAY A, Y	Y+A→Y	Adds 8-bit A accumulator to Y
LEAY D, Y	Y+D→Y	Adds 16-bit D accumulator to Y
LEAU-10, U	U-10→U	Subtracts 10 from U
LEAS-10, S	S-10→S	Used to reserve area on stack
LEAS 10, S	S+10→S	Used to 'clean up' stack
LEAX 5, S	S+5→X	Transfers as well as adds

- LEAa, -b
 1. b -1→temp (calculate EA with predecrement)
 2. b -1→b (modify b, predecrement)
 3. temp→a (load a)

Autoincrement-by-two and autodecrement-by-two instructions work similarly. Note that LEAX, X+ does not change X, however LEAX, -X does decrement X. LEAX 1, X should be used to increment X by one.

MUL

Multiplies the unsigned binary numbers in the A and B accumulator and places the unsigned result into the 16-bit D accumulator. This unsigned multiply also allows multiple-precision multiplications.

Long And Short Relative Branches

The HD6309 has the capability of program counter relative branching throughout the entire memory map. In this mode, if the branch is to be taken, the 8-or 16-bit signed offset is added to the value of the program counter to be used as the effective address.

This allows the program to branch anywhere in the 64k memory map. Position independent code can be easily generated through the use of relative branching. Both short (8-bit) and long (16-bit) branches are available.

SYNC

After encountering a sync instruction, the MPU enters a sync state, stops processing instructions, and waits for an interrupt. If the pending interrupt is non-maskable (NMI) or maskable (FIRQ, IRQ) with its mask bit (F or I) clear, the processor will clear the sync state and perform the normal interrupt stacking and service routine. Since FIRQ and IRQ are not edge-triggered, a low level with a minimum duration of three bus cycles is required to assure that the interrupt will be taken. If the pending interrupt is maskable (FIRQ, IRQ) with its mask bit (F or I) set, the processor will clear the sync state and continue processing by executing the next inline instruction. Figure 19 depicts sync timing.

Software Interrupt

A software interrupt instruction will cause an interrupt, and its associated vector fetch.

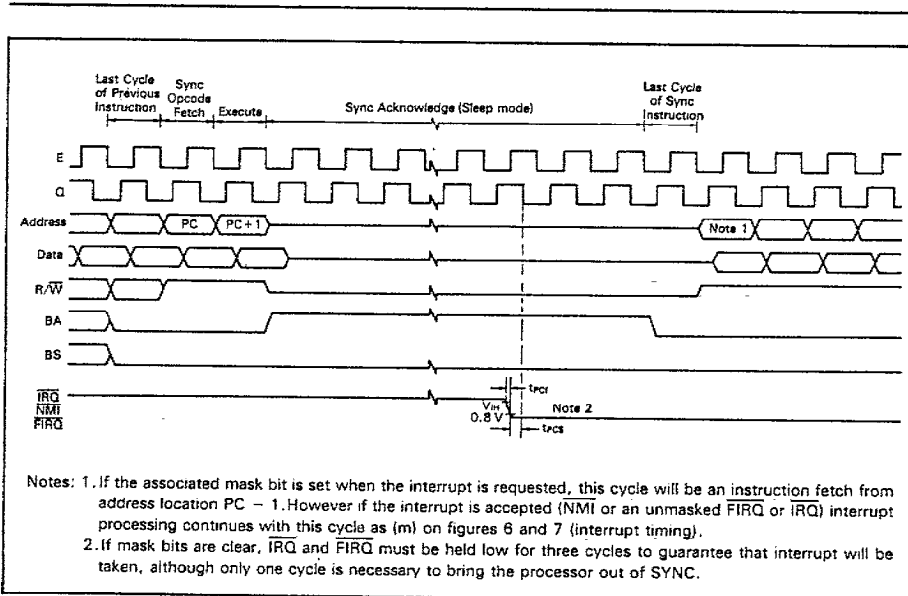


Figure 19. Sync Timing

These software interrupts are useful in operating system calls, software debugging, trace operations, memory mapping, and software development systems. Three levels of SWI are available on this HD6309, and are prioritized in the following order: SWI, SWI2, SWI3.

16-Bit Operation

The HD6309 has the capability of processing 16-bit data. These instructions include loads, stores, compares, adds, subtracts, transfers, exchanges, pushes and pulls.

Cycle-by-Cycle Operation

The address bus cycle-by-cycle performance chart illustrates the memory-access sequence corresponding to each possible instruction and addressing mode in the HD6309. Each instruction begins with an opcode fetch. While that opcode is being internally decoded, the next program byte is always fetched. (Most instructions will use the next byte, so this technique considerably speeds throughput.) Next, the operation of each opcode will follow the flow chart. VMA is an indication of FFFF₁₆ on the address bus, R/W = high and BS = low. The following examples illustrate the use of the chart: see figure 20.

Example 1: LBSR (Branch Taken)

Before Execution SP = F000

		.	
		.	
\$8000		LBSR	CAT
		.	
		.	
\$A000	CAT	.	

Cycle-by-Cycle Flow

Cycle	Address	Data	R/W	Description
1	8000	17	1	Opcode Fetch
2	8001	1F	1	Offset High Byte
3	8002	FD	1	Offset Low Byte
4	FFFF	*	1	VMA Cycle
5	FFFF	*	1	VMA Cycle
6	FFFF	*	1	VMA Cycle
7	FFFF	*	1	VMA Cycle
8	FFFF	03	0	Stack Low Order Byte of Return Address
9	EFEE	80	0	Stack High Order Byte of Return Address

Example 2: DEC (Extended)

\$8000	DEC	\$A000
\$A000	FCB	\$80

Cycle-by-Cycle Flow

Cycle	Address	Data	R/W	Description
1	8000	7A	1	Opcode Fetch
2	8001	A0	1	Operand Address, High Byte
3	8002	00	1	Operand Address, Low Byte
4	FFFF	*	1	VMA Cycle
5	A000	80	1	Read the Data
6	FFFF	*	1	VMA Cycle
7	A000	7F	0	Store the De- cremented Data

* The data bus has the data at that particular address.

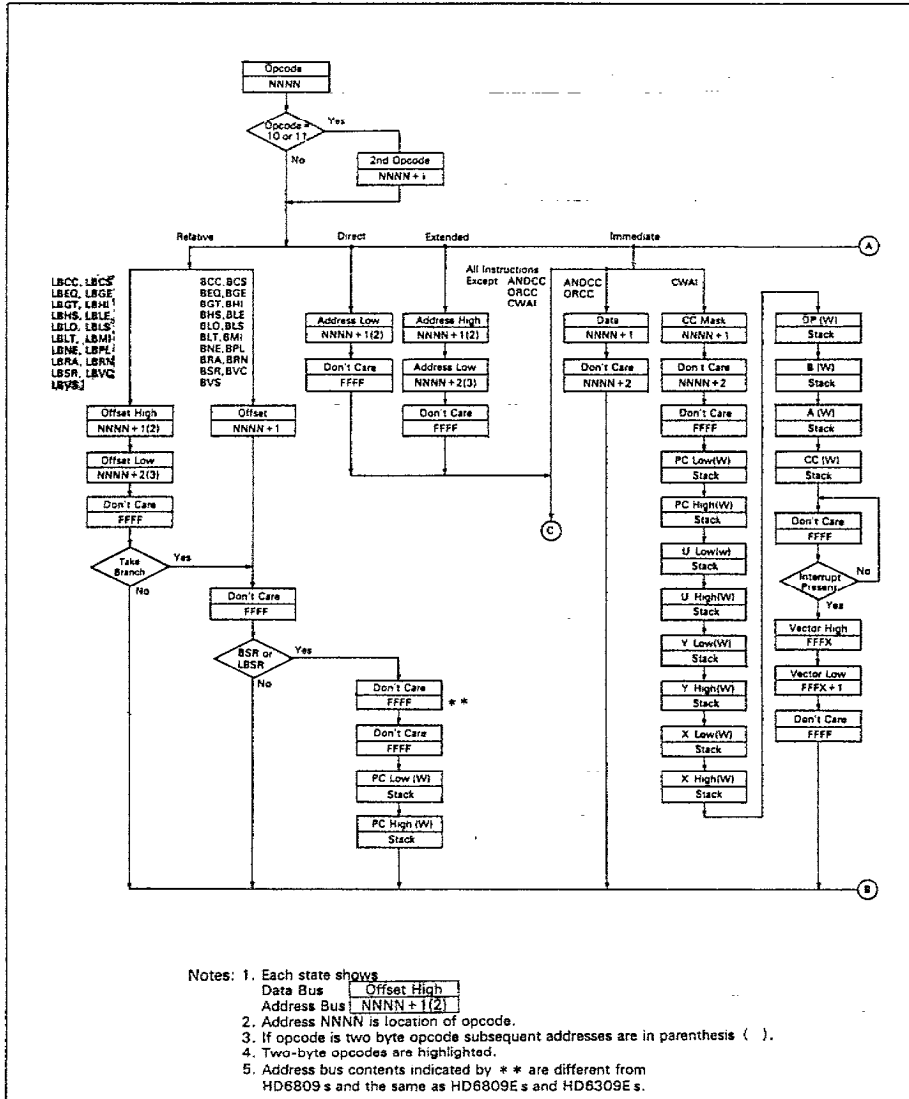


Figure 20. Cycle-by-Cycle Performance

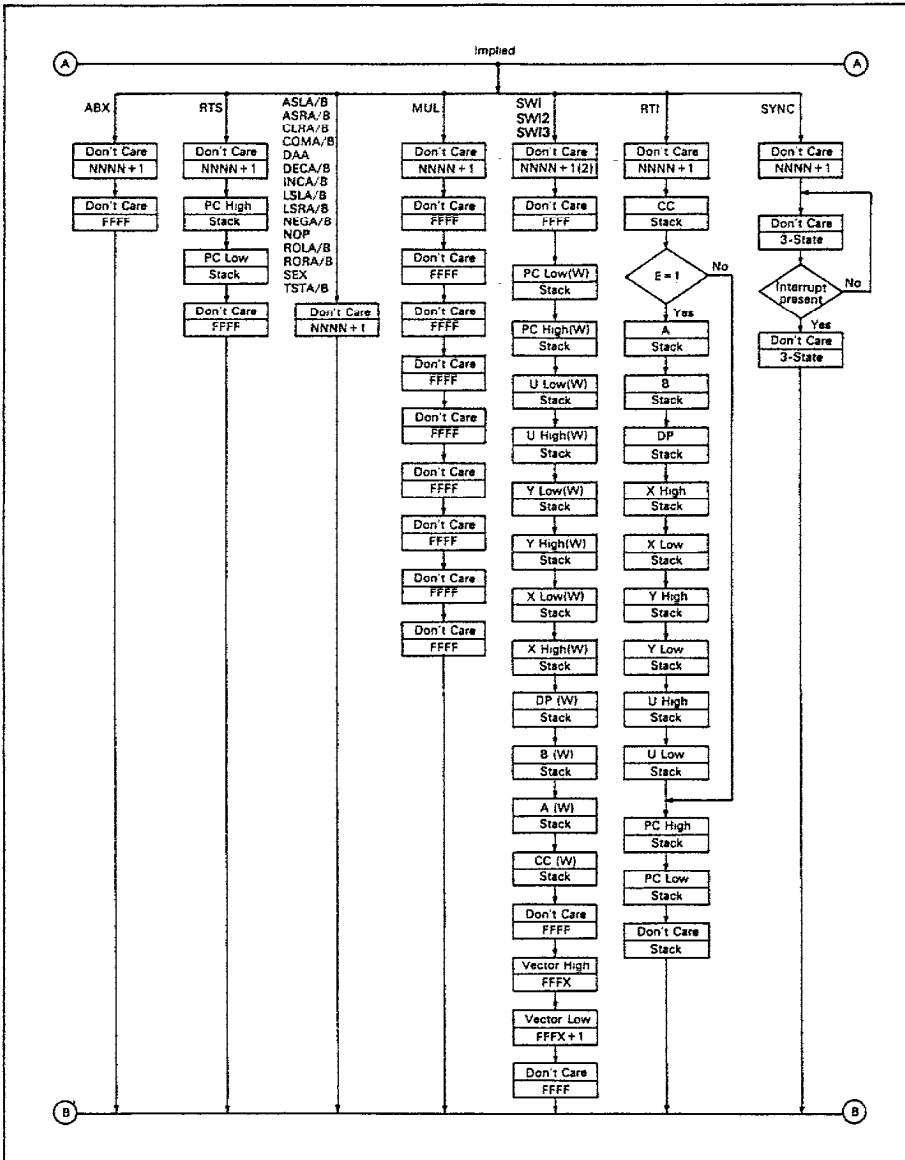


Figure 20. Cycle-by-Cycle Performance (Cont.)

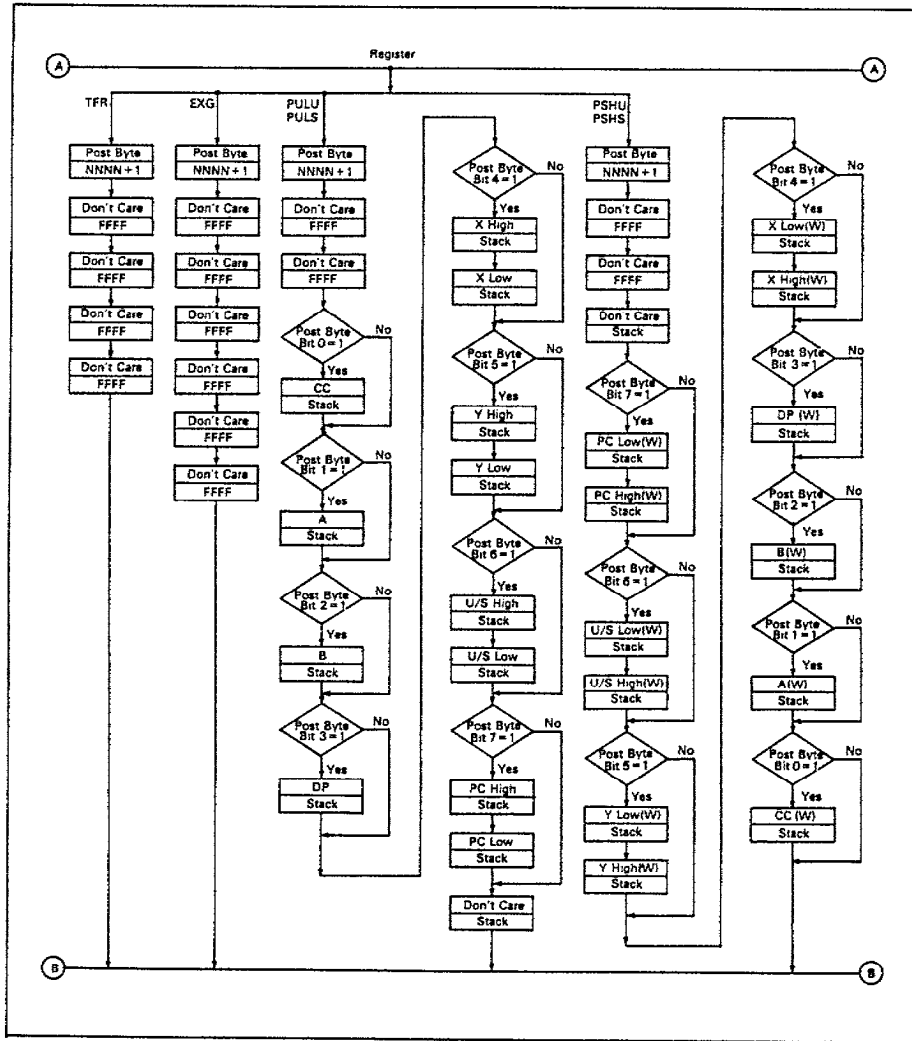


Figure 20. Cycle-by-Cycle Performance (Cont.)

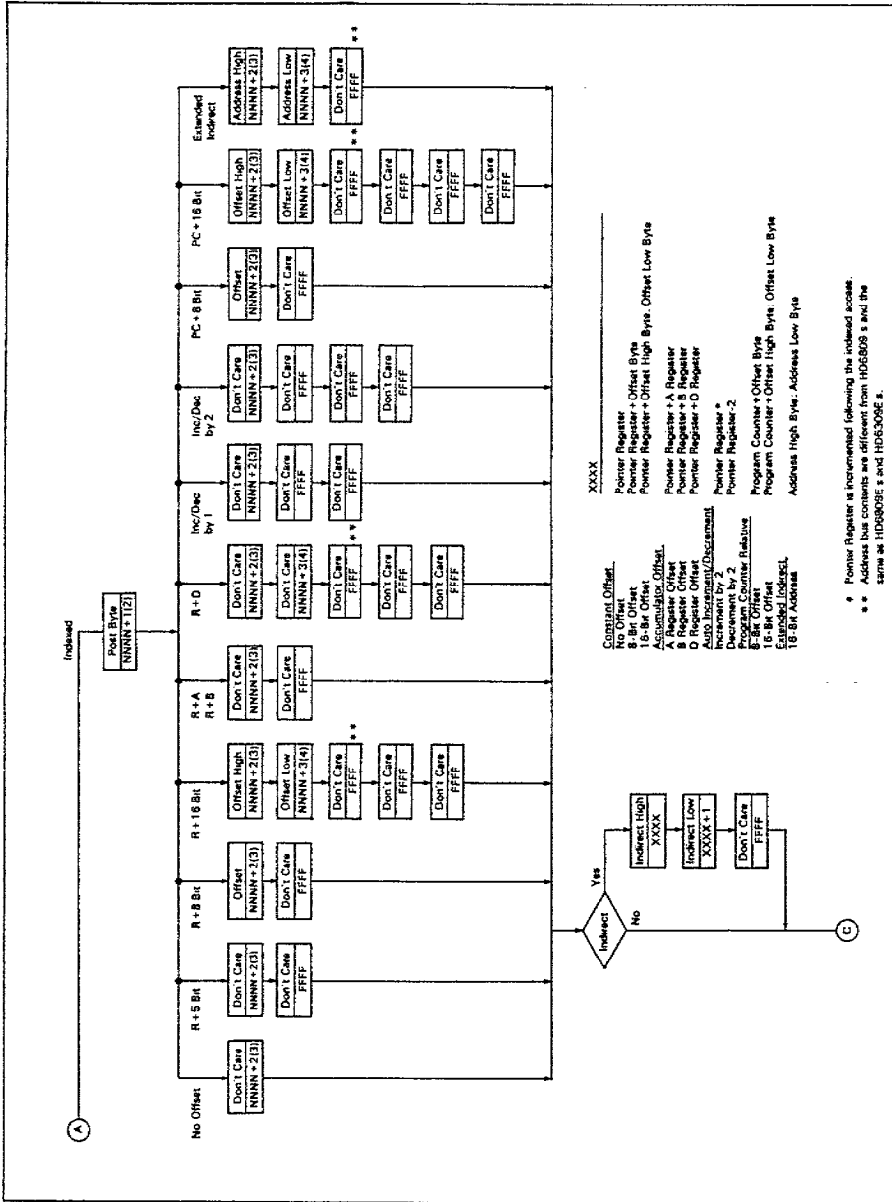


Figure 20. Cycle-by-Cycle Performance (Cont.)

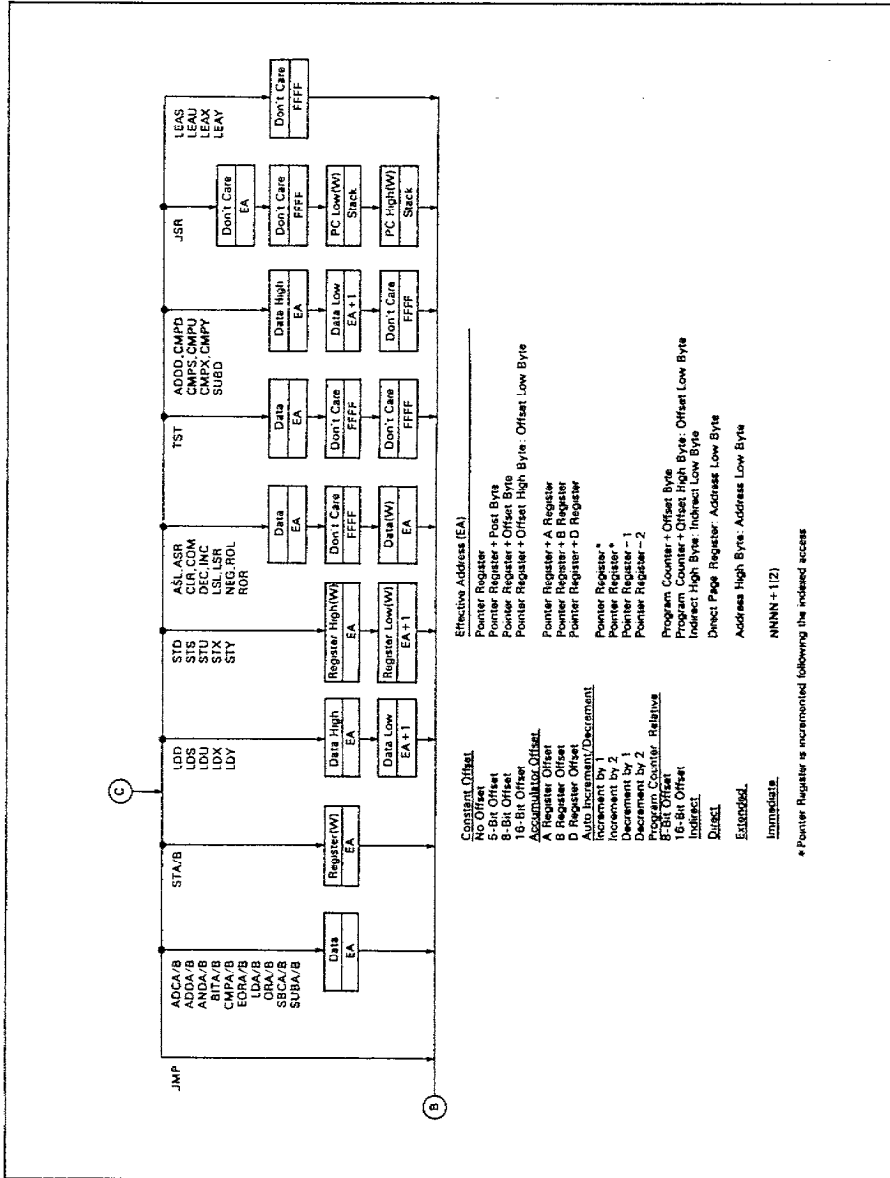


Figure 20. Cycle-by-Cycle Performance (Cont.)

Sleep Mode

During the interrupt wait period in the SYNC instruction (the sync state) and in the CWAI instruction (the wait state), MPU operation is halted and goes to the sleep mode. However, the state of I/O pins is the same as that of the HD6809 in this mode.

HD6309 Instruction set Tables

The instructions of the HD6309 have been broken down into five different categories. They are as follows:

- 8-Bit operation (table 6)
- 16-Bit operation (table 7)
- Index register/stack pointer instructions (table 8)
- Relative branches (long or short) (table 9)
- Miscellaneous instructions (table 10)

HD6309 instruction set tables and Hexadecimal Values of instructions are shown in table 11 and table 12.

Table 6. 8-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADCA, ADCB	Add memory to accumulator with carry
ADDA, ADDB	Add memory to accumulator
ANDA, ANDB	AND memory with accumulator
ASL, ASLA, ASLB	Arithmetic shift of accumulator or memory left
ASR, ASRA, ASRB	Arithmetic shift of accumulator or memory right
BITA, BITB	Bit test memory with accumulator
CLR, CLRA, CLRB	Clear accumulator or memory location
CMPA, CMPB	Compare memory from accumulator
COM, COMA, COMB	Complement accumulator or memory location
DAA	Decimal adjust A accumulator
DEC, DECA, DECB	Decrement accumulator or memory location
EORA, EORB	Exclusive OR memory with accumulator
EXG R1, R2	Exchange R1 with R2 (R1, R2=A, B, CC, DP)
INC, INCA, INCB	Increment accumulator or memory location
LDA, LDB	Load accumulator from memory
LSL, LSLA, LSLB	Logical shift left accumulator or memory location
LSR, LSRA, LSRB	Logical shift right accumulator or memory location
MUL	Unsigned multiply (A × B → D)
NEG, NEGA, NEGB	Negate accumulator or memory
ORA, ORB	OR memory with accumulator
ROL, ROLA, ROLB	Rotate accumulator or memory left
ROR, RORA, RORB	Rotate accumulator or memory right
SBCA, SBCB	Subtract memory from accumulator with borrow
STA, STB	Store accumulator to memory
SUBA, SUBB	Subtract memory from accumulator
TST, TSTA, TSTB	Test accumulator or memory location
TFR R1, R2	Transfer R1 or R2 (R1, R2=A, B, CC, DP)

Note: A, B, CC or DP may be pushed to (pulled from) either stack with PSHS, PSHU (PULS, PULU) instructions.

Table 7. 16-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADDD	Add memory to D accumulator
CMPD	Compare memory from D accumulator
EXG D, R	Exchange D with X, Y, S, U or PC
LDD	Load D accumulator from memory
SEX	Sign Extend B accumulator into A accumulator
STD	Store D accumulator to memory
SUBD	Subtract memory from D accumulator
TFR D, R	Transfer D to X, Y, S, U or PC
TFR R, D	Transfer X, Y, S, U or PC to D

Note: D may be pushed (pulled) to either stack with PSHS, PSHU (PULS, PULU) instructions.

Table 8. Index Register/Stack Pointer Instructions

Mnemonic(s)	Operation
CMPS, CMPU	Compare memory from stack pointer
CMPX, CMPY	Compare memory from index register
EXG R1, R2	Exchange D, X, Y, S, U or PC with D, X, Y, S, U or PC
LEAS, LEAU	Load effective address into stack pointer
LEAX, LEAY	Load effective address into index register
LDS, LDU	Load stack pointer from memory
LDX, LDY	Load index register from memory
PSHS	Push A, B, CC, DP, D, X, Y, U or PC onto hardware stack
PSHU	Push A, B, CC, DP, D, X, Y, S or PC onto user stack
PULS	Pull A, B, CC, DP, D, X, Y, U or PC from hardware stack
PULU	Pull A, B, CC, DP, D, X, Y, S or PC from user stack
STS, STU	Store stack pointer to memory
STX, STY	Store index register to memory
TFR R1, R2	Transfer D, X, Y, S, U or PC to D, X, Y, S, U or PC
ABX	Add B accumulator to X (unsigned)

Table 9. Branch Instructions

Mnemonic(s)	Operation
Simple Branches	
BEQ, LBEQ	Branch if equal
BNE, LBNE	Branch if not equal
BMI, LBMI	Branch if minus
BPL, LBPL	Branch if plus
BCS, LBCCS	Branch if carry set
BCC, LBCC	Branch if carry clear
BVS, LBVS	Branch if overflow set
BVC, LBVC	Branch if overflow clear
Signed Branches	
BGT, LBGT	Branch if greater (signed)
BGE, LBGE	Branch if greater than or equal (signed)
BEQ, LBEQ	Branch if equal
BLE, LBLE	Branch if less than or equal (signed)
BLT, LBLT	Branch if less than (signed)
Unsigned Branches	
BHI, LBHI	Branch if higher (unsigned)
BHS, LBHS	Branch if higher or same (unsigned)
BEQ, LBEQ	Branch if equal
BLS, LBLS	Branch if lower or same (unsigned)
BLO, LBLO	Branch if lower (unsigned)
Other Branches	
BSR, LBSR	Branch to subroutine
BRA, LBRA	Branch always
BRN, LBRN	Branch never

Table 10. Miscellaneous Instructions

Mnemonic(s)	Operation
ANDCC	AND condition code register
CWAI	AND condition code register, then wait for interrupt
NOP	No operation
ORCC	OR condition code register
JMP	Jump
JSR	Jump to subroutine
RTI	Return from interrupt
RTS	Return from subroutine
SWI, SWI2, SWI3	Software interrupt (absolute indirect)
SYNC	Synchronize with interrupt line

Table 11. HD6309 Instruction Set

Instruction/ Forms	HD6309 Addressing Modes						Description	5 3 2 1 0				
	Implied	Direct	Extended	Immediate	Indexed	Relative		H	N	Z	V	C
	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #						
ABX	3A 3 1						B + X - X (Unsigned)	•	•	•	•	•
ADC ADCA ADCB		99 4 2 D9 4 2	B9 5 3 F9 5 3	89 2 2 C9 2 2	A9 4+ 2+ E9 4+ 2+		A + M + C - A B + M + C - B	•	•	•	•	•
ADD ADDA ADDB ADDD		9B 4 2 DB 4 2 D3 6 2	BB 5 3 FB 5 3 F3 7 3	8B 2 2 CB 2 2 C3 4 3	AB 4+ 2+ EB 4+ 2+ E3 6+ 2+		A + M - A B + M - B D + M; M + 1 - D	•	•	•	•	•
AND ANDA ANDB ANDCC		94 4 2 D4 4 2	B4 5 3 F4 5 3	84 2 2 C4 2 2 1C 3 2	A4 4+ 2+ E4 4+ 2+		A * M - A B * M - B CC IMM - CC	•	•	•	•	•
ASL ASLA ASLB ASL	48 2 1 58 2 1					68 6+ 2+	A B M / C b7 b0	•	•	•	•	•
ASR ASRA ASRB ASR	47 2 1 57 2 1					67 6+ 2+	A B M / b7 b0 C	•	•	•	•	•
BCC BCC LBCC						24 3 2 10 5.6 4 24	Branch C = 0 Long Branch C = 0	•	•	•	•	•
BCS BCS LBCS						25 3 2 10 5.6 4 25	Branch C = 1 Long Branch C = 1	•	•	•	•	•
BEQ BEQ LBEQ						27 3 2 10 5.6 4 27	Branch Z = 1 Long Branch Z = 1	•	•	•	•	•
BGE BGE LBGE						2C 3 2 10 5.6 4 2C	Branch N&V = 0 Long Branch N&V = 0	•	•	•	•	•
BGT BGT LBGT						2E 3 2 10 5.6 4 2E	Branch Z, (N&V) = 0 Long Branch Z, (N&V) = 0	•	•	•	•	•
BHI BHI LBHI						22 3 2 10 5.6 4 22	Branch C, Z = 0 Long Branch C, Z = 0	•	•	•	•	•
BHS BHS LBHS						24 3 2 10 5.6 4 24	Branch C = 0 Long Branch C = 0	•	•	•	•	•
BIT BITA BITB		95 4 2 D5 4 2	B5 5 3 F5 5 3	85 2 2 C5 2 2	A5 4+ 2+ E5 4+ 2+		Bit Test A(M : A) Bit Test B(M : B)	•	•	•	•	•
BLE BLE LBLE						2F 3 2 10 5.6 4 2F	Branch Z, (N&V) = 1 Long Branch Z, (N&V) = 1	•	•	•	•	•
BLO BLO LBLO						25 3 2 10 5.6 4 25	Branch C = 1 Long Branch C = 1	•	•	•	•	•
BLS BLS LBLS						23 3 2 10 5.6 4 23	Branch C, Z = 1 Long Branch C, Z = 1	•	•	•	•	•
BLT BLT LBLT						2D 3 2 10 5.6 4 2D	Branch N&V = 1 Long Branch N&V = 1	•	•	•	•	•
BMI BMI LBMI						2B 3 2 10 5.6 4 2B	Branch N = 1 Long Branch N = 1	•	•	•	•	•

Table 11. HD6309 Instruction Set (Cont.)

Instruction: Forms	HD6309 Addressing Modes						Description	5 3 2 1 0				
	Implied	Direct	Extended	Immediate	Indexed ¹	Relative		H	N	Z	V	C
	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #						
BNE BNE LBNE						26 3 2 10 5.6: 4 28	Branch Z=0 Long Branch Z=0	•	•	•	•	•
BPL BPL LBPL						2A 3 2 10 5.6: 4 2A	Branch N=0 Long Branch N=0	•	•	•	•	•
BRA BRA LBRA						20 3 2 16 5 3	Branch Always Long Branch Always	•	•	•	•	•
BRN BRN LBRN						21 3 2 10 5 4 21	Branch Never Long Branch Never	•	•	•	•	•
BSR BSR LBSR						8D 7 2 17 9 3	Branch to Subroutine Long Branch to Subroutine	•	•	•	•	•
BVC BVC LBVC						28 3 2 10 5.6: 4 28	Branch V=0 Long Branch V=0	•	•	•	•	•
BVS BVS LBVS						29 3 2 10 5.6: 4 29	Branch V=1 Long Branch V=1	•	•	•	•	•
CLR CLRA CLRB CLR	4F 2 1 5F 2 1						0-A 0-B 0-M	•	0	1	0	0
CMP CMPA CMPB CMPD CMPF CMPH CMPL CMPQ CMPR CMPS CMPU CMPX CMPY		91 4 2 D1 4 2 10 7 3 93 11 7 3 9C 11 7 3 93 9C 10 7 3 9C	B1 5 3 F1 5 3 10 8 4 B3 11 8 4 BC 11 8 4 B3 BC 10 8 4 BC	81 2 2 C1 2 2 10 5 4 83 11 5 4 8C 11 5 4 83 8C 10 5 4 8C	A1 4+ 2+ E1 4+ 2+ 10 7+ 3+ A3 11 7+ 3+ AC 11 7+ 3+ A3 AC 10 7+ 3+ AC		Compare M from A Compare M from B Compare M:M+1 from D Compare M:M+1 from S Compare M:M-1 from U Compare M:M-1 from X Compare M:M-1 from Y	•	:	:	:	:
COM COMA COMB COM	43 2 1 53 2 1	03 6 2	73 7 3		63 6+ 2+		A-A B-B M-M	•	:	:	0	1
CWAI				3C 20 2			CC IMM-CC (except 1-E)	—	—	—	—	—
DAA	19 2 1						Wait for Interrupt Decimal Adjust A	•	:	:	:	:
DEC DECA DECB DEC	4A 2 1 5A 2 1	0A 6 2	7A 7 3		6A 6+ 2+		A-1-A B-1-B M-1-M	•	:	:	:	•
EOR EORA EORB		98 4 2 08 4 2	B8 5 3 F8 5 3	88 2 2 C8 2 2	A8 4+ 2+ E8 4+ 2+		A ⊕ M-A B ⊕ M-B	•	:	:	0	•
EXG R1, R2	1E 7 2						R1-R2	—	—	—	—	—
INC INCA INCB INC	4C 2 1 5C 2 1	0C 6 2	7C 7 3		6C 6+ 2+		A+1-A B+1-B M+1-M	•	:	:	:	•
JMP		0E 3 2	7E 4 3		6E 3+ 2+		EA ³ -PC	•	•	•	•	•
JSR		9D 7 2	BD 8 3		AD 7+ 2+		Jump to Subroutine	•	•	•	•	•

Table 11. HD6309 Instruction Set (Cont.)





Instruction/ Forms	HD6309 Addressing Modes						Description					
	Implied	Direct	Extended	Immediate	Indexed	Relative		5	3	2	1	0
	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #		H	N	Z	V	C
LD LDA LDB LDD LDS		96 4 2	B6 5 3	86 2 2	A6 4+ 2+		M-A	•	•	•	•	•
		D6 4 2	F6 5 3	C6 2 2	E6 4+ 2+		M-B	•	•	•	•	•
		DC 5 2	FC 6 3	CC 3 3	EC 5+ 2+		M:M+1-D	•	•	•	•	•
		10 6 3	10 7 4	10 4 4	10 6+ 3+		M:M+1-S	•	•	•	•	•
		DE 5 2	FE 6 3	CE 3 3	EE 5+ 2+		M:M+1-U	•	•	•	•	•
LDU LDX LDY		DE 5 2	FE 6 3	CE 3 3	EE 5+ 2+		M:M+1-U	•	•	•	•	•
		9E 5 2	BE 6 3	8E 3 3	AE 5+ 2+		M:M+1-X	•	•	•	•	•
		10 6 3	10 7 4	10 4 4	10 6+ 3+		M:M+1-Y	•	•	•	•	•
LEA LEAS LEAU LEAX LEAY					32 4+ 2+		EA ³ -S	•	•	•	•	•
					33 4+ 2+		EA ³ -U	•	•	•	•	•
					30 4+ 2+		EA ³ -X	•	•	•	•	•
					31 4+ 2+		EA ³ -Y	•	•	•	•	•
LSL LSLA LSLB LSL	48 2 1 58 2 1							•	•	•	•	•
		08 6 2	78 7 3		68 6+ 2+			•	•	•	•	•
LSR LSRA LSRB LSR	44 2 1 54 2 1							•	•	•	•	•
		04 6 2	74 7 3		64 6+ 2+			•	•	•	•	•
MUL	3D 11 1						A x B-D (Unsigned)	•	•	•	•	•
NEG NEGA NEGB NEG	40 2 1 50 2 1						$\bar{A}+1-A$ $\bar{B}+1-B$ M+1-M	•	•	•	•	•
		00 6 2	70 7 3		60 6+ 2+			•	•	•	•	•
NOP	12 2 1						No Operation	•	•	•	•	•
OR ORA ORB ORCC		9A 4 2 DA 4 2	BA 5 3 FA 5 3	8A 2 2 CA 2 2 1A 3 2	AA 4+ 2+ EA 4+ 2+		A, M-A B, M-B CC, IMM-CC	•	•	•	•	•
	34 5+ 2 36 5+ 2						Push Registers on S Stack Push Registers on U Stack	•	•	•	•	•
	35 5+ 2 37 5+ 2						Pull Registers from S Stack Pull Registers from U Stack	•	•	•	•	•
ROL ROLA ROLB ROL	49 2 1 59 2 1							•	•	•	•	•
		09 6 2	79 7 3		69 6+ 2+			•	•	•	•	•
ROR RORA RORB ROR	46 2 1 56 2 1							•	•	•	•	•
		06 6 2	76 7 3		66 6+ 2+			•	•	•	•	•
RTI	3B 6 1 5 1						Return from Interrupt	•	•	•	•	•
RTS	39 5 1						Return from Subroutine	•	•	•	•	•
SBC SBCA SBCB		92 4 2 D2 4 2	82 5 3 F2 5 3	82 2 2 C2 2 2	A2 4+ 2+ E2 4+ 2+		A-M-C-A B-M-C-B	•	•	•	•	•
	1D 2 1						Sign Extend B into A	•	•	•	•	•
ST STA STB STD STS		97 4 2	B7 5 3		A7 4+ 2+		A-M	•	•	•	•	•
		D7 4 2	F7 5 3		E7 4+ 2+		B-M	•	•	•	•	•
		DD 5 2	FD 6 3		ED 5+ 2+		D-M:M+1	•	•	•	•	•
		10 6 3	10 7 4		10 6+ 3+		S-M:M+1	•	•	•	•	•
		DF 5 2	FF 6 3		EF 5+ 2+		U-M:M+1	•	•	•	•	•
		9F 5 2	BF 6 3		AF 5+ 2+		X-M:M+1	•	•	•	•	•
		10 6 3	10 7 4		10 6+ 3+		Y-M:M+1	•	•	•	•	•
		9F 5 2	BF 6 3		AF 5+ 2+			•	•	•	•	•

Table 11. HD6309 Instruction Set (Cont.)

Instruction/ Forms	HD6309 Addressing Modes							Description	5 3 2 1 0				
	Implied	Direct	Extended	Immediate	Indexed ¹	Relative	H		N	Z	V	C	
	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #	OP ~ #							
SUB SUBA SUBB SUBD		90 4 2 D0 4 2 93 6 2	B0 5 3 F0 5 3 B3 7 3	80 2 2 C0 2 2 83 4 3	A0 4+ 2+ E0 4+ 2+ A3 6+ 2+		A-M-A B-M-B D-M:M+1-D	1	:	:	:	:	
SWI SWI ⁵ SWI2 ⁵ SWI3 ⁵	3F 19 1 10 20 2 3F 11 20 2 3F						Software Interrupt 1 Software Interrupt 2 Software Interrupt 3	●	●	●	●	●	
SYNC	13 24 1						Synchronize to Interrupt	●	●	●	●	●	
TFR R1, R2	1F 6 2						R1-R2 ²	← 6 →					
TST TSTA TSTB TST	4D 2 1 5D 2 1	0D 6 2 7D 7 3			6D 6+ 2+		Test A Test B Test M	●	1	:	0	●	

- Legend: OP Operation Code (Hexadecimal) Z Zero (byte)
 ~ Number of MPU Cycles V Overflow, 2's complement
 # Number of Program Bytes C Carry from bit 7
 + Arithmetic Plus I Test and set if true, cleared otherwise
 - Arithmetic Minus ● Not Affected
 X Multiply CC Condition Code Register
 M Complement of M : Concatenation
 → Transfer Into V Logical or
 H Half-carry (from bit 3) ^ Logical and
 N Negative (sign bit) ⊕ Logical Exclusive or

- Notes: ① This column gives a base cycle and byte count. To obtain total count, and the values obtained from the Indexed Addressing Modes table.
 ② R1 and R2 may be any pair of 8-bit or any pair of 16-bit registers.
 The 8-bit registers are: A, B, CC, DP
 The 16-bit registers are: X, Y, U, S, D, PC
 ③ EA is the effective address.
 ④ The PSH and PUL instructions require 5 cycle plus 1 cycle for each byte pushed or pulled.
 ⑤ 5(b) means: 5 cycles if branch not taken, 6 cycles if taken.
 ⑥ SWI sets I and F bits. SWI2 and SWI3 do not affect I and F.
 ⑦ Conditions Codes set as a direct result of the instruction.
 ⑧ Value of half-carry flag is undefined.
 ⑨ Special Case—Carry set if b7 is SET.
 ⑩ Condition Codes set as a direct result of the instruction if CC is specified, and not affected otherwise.

Table 12. Hexadecimal Values of Machine Codes

OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#
00	NEG	Direct	6	2	30	LEAX	Indexed	4+	2+	60	NEG	Indexed	6+	2+
01	*	↑			31	LEAY	↑	4+	2+	61	*	↑		
02	*				32	LEAS	↓	4+	2+	62	*			
03	COM		6	2	33	LEAU	Indexed	4+	2+	63	COM		6+	2+
04	LSR		6	2	34	PSHS	Implied	5+	2	64	LSR		6+	2+
05	*				35	PULS	↑	5+	2	65	*			
06	ROR		6	2	36	PSHU	↑	5+	2	66	ROR		6+	2+
07	ASR		6	2	37	PULU	↑	5+	2	67	ASR		6+	2+
08	ASL, LSL		6	2	38	*				68	ASL, LSL		6+	2+
09	ROL		6	2	39	RTS		5	1	69	ROL		6+	2+
0A	DEC		6	2	3A	ABX	↓	3	1	6A	DEC		6+	2+
0B	*				3B	RTI	Implied	6, 15	1	6B	*			
0C	INC		6	2	3C	CWAI	Immed	≥20	2	6C	INC		6+	2+
0D	TST		6	2	3D	MUL	Implied	11	1	6D	TST		6+	2+
0E	JMP		3	2	3E	*				6E	JMP		3+	2+
0F	CLR	Direct	6	2	3F	SWI	Implied	19	1	6F	CLR	Indexed	6+	2+
10	See	-	-	-	40	NEGA	Implied	2	1	70	NEG	Extended	7	3
11	Next Page	-	-	-	41	*	↑			71	*	↑		
12	NOP	Implied	2	1	42	*				72	*			
13	SYNC	Implied	≥4	1	43	COMA		2	1	73	COM		7	3
14	*				44	LSRA		2	1	74	LSR		7	3
15	*				45	*				75	*			
16	LBRA	Relative	5	3	46	RORA		2	1	76	ROR		7	3
17	LBSR	Relative	9	3	47	ASRA		2	1	77	ASR		7	3
18	*				48	ASLA, LSLA		2	1	78	ASL, LSL		7	3
19	DAA	Implied	2	1	49	ROLA		2	1	79	ROL		7	3
1A	ORCC	Immed	3	2	4A	DECA		2	1	7A	DEC		7	3
1B	*				4B	*				7B	*			
1C	ANDCC	Immed	3	2	4C	INCA		2	1	7C	INC		7	3
1D	SEX	Implied	2	1	4D	ISTA		2	1	7D	TST		7	3
1E	EXG	↓	8	2	4E	*				7E	JMP		4	3
1F	TFR	Implied	6	2	4F	CLRA	Implied	2	1	7F	CLR	Extended	7	3
20	BRA	Relative	3	2	50	NEGB	Implied	2	1	80	SUBA	Immed	2	2
21	BRN		3	2	51	*	↑			81	CMPA		2	2
22	BHI		3	2	52	*				82	SBCA		2	2
23	BLS		3	2	53	COMB		2	1	83	SUBD		4	3
24	BHS, BCC		3	2	54	LSRB		2	1	84	ANDA		2	2
25	BLO, BCS		3	2	55	*				85	BITA		2	2
26	BNE		3	2	56	RORB		2	1	86	LDA		2	2
27	BEQ		3	2	57	ASRB		2	1	87	*			
28	BVC		3	2	58	ASLB, LSLB		2	1	88	EORA		2	2
29	BVS		3	2	59	ROLB		2	1	89	ADCA		2	2
2A	BPL		3	2	5A	DECB		2	1	8A	ORA		2	2
2B	BMI		3	2	5B	*				8B	ADDA		2	2
2C	BGE		3	2	5C	INCB		2	1	8C	CMPX	Immed	4	3
2D	BLT		3	2	5D	TSTB		2	1	8D	BSR	Relative	7	2
2E	BGT		3	2	5E	*	↓			8E	LDX	Immed	3	3
2F	BLE	Relative	3	2	5F	CLRB	Implied	2	1	8F	*			

Legend: ~ Number of MPU cycles (less possible push pull or indexed-mode cycles)
 # Number of program bytes
 * Denotes unused opcode

Table 12. Hexadecimal Values of Machine Codes (Cont.)

OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#		
90	SUBA	Direct	4	2	C6	LDB	Immed	2	2	FC	LDD	Extended	6	3		
91	CMPA	↑	4	2	C7	*	↑			FD	STD	↑	6	3		
92	SBCA		4	2	C8	EORB		2	2	FE	LDU		6	3		
93	SUBD	↓	6	2	C9	ADCB	↓			FF	STU	↓	Extended	6	3	
94	ANDA		4	2	CA	ORB		2	2							
95	BITA	↓	4	2	CB	ADDB	↓			2 Bytes Opcode						
96	LDA		4	2	CC	LDD		3	3							
197	STA	↓	4	2	CD	*	↓			1021	LBRN	↑	Relative	5	4	
98	EORA		4	2	CE	LDU		Immed	3	3	1022		LBHI	5	4	
99	ADCA	↓	4	2	CF	*	↓			1023	LBLS	↑	5	4		
9A	ORA		4	2						1024	LBHS, LBCC		5	4		
9B	ADDA	↓	4	2	D0	SUBB	↑	Direct	4	2	1025	LBCS, LBLO	↑	5	4	
9C	CMPX		6	2	D1	CMPB		4	2	1026	LBNE	5		4		
9D	JSR	↓	7	2	D2	SBCB	↑			1027	LBEQ	↑	5	4		
9E	LDX		5	2	D3	ADDD		6	2	1028	LBVC		5	4		
9F	STX	Direct	5	2	D4	ANDB	↑			1029	LBVS	↑	5	4		
					D5	BITB		4	2	102A	LBPL		5	4		
A0	SUBA	↑	4+	2+	D6	LDB	↓			102B	LBMI	↑	5	4		
A1	CMPA		4+	2+	D7	STB		4	2	102C	LBGE		5	4		
A2	SBCA	↑	4+	2+	D8	EORB	↓			102D	LBLT	↑	5	4		
A3	SUBD		6+	2+	D9	ADCB		4	2	102E	LBGT		5	4		
A4	ANDA	↓	4+	2+	DA	ORB	↑			102F	LBLE	↑	Relative	5	4	
A5	BITA		4+	2+	DB	ADDB		4	2	103F	SWI2		Implied	20	2	
A6	LDA	↓	4+	2+	DC	LDD	↓			1083	CMPD	↑	Immed	5	4	
A7	STA		4+	2+	DD	STD		5	2	108C	CMPY		5	4		
A8	EORA	↓	4+	2+	DE	LDU	↑			108E	LDY	↑	Immed	4	4	
A9	ADCA		4+	2+	DF	STU		Direct	5	2	1093		CMPD	Direct	7	3
AA	ORA	↓	4+	2+	E0	SUBB	↑	Indexed	4+	2+	109C	CMPY	↑	7	3	
AB	ADDA		4+	2+	E1	CMPB		4+	2+	109E	LDY	6		3		
AC	CMPX	↓	6+	2+	E2	SBCB	↑			109F	STY	↑	Direct	6	3	
AD	JSR		7+	2+	E3	ADDD		6+	2+	10A3	CMPD		Indexed	7+	3+	
AE	LDX	↓	5+	2+	E4	ANDB	↑			10AC	CMPY	↑	7+	3+		
AF	STX		Indexed	5+	2+	E5		BITB	4+	2+	10AE		LDY	6+	3+	
B0	SUBA	↑	5	3	E6	LDB	↓			10AF	STY	↑	Indexed	6+	3+	
B1	CMPA		5	3	E7	STB		4+	2+	10B3	CMPD		Extended	8	4	
B2	SBCA	↑	5	3	E8	EORB	↓			10B8	CMPY	↑	8	4		
B3	SUBD		7	3	E9	ADCB		4+	2+	10BE	LDY		7	4		
B4	ANDA	↓	5	3	EA	ORB	↑			10BF	STY	↑	Extended	7	4	
B5	BITA		5	3	EB	ADDB		4+	2+	10CE	LDS		Immed	4	4	
B6	LDA	↓	5	3	EC	LDD	↑			10DE	LDS	↑	Direct	6	3	
B7	STA		5	3	ED	STD		5+	2+	10DF	STS		Direct	6	3	
B8	EORA	↓	5	3	EE	LDU	↑			10EE	LDS	↑	Indexed	6+	3+	
B9	ADCA		5	3	EF	STU		Indexed	5+	2+	10EF		STS	Indexed	6+	3+
BA	ORA	↓	5	3	F0	SUBB	↑	Extended	5	3	10FE	LDS	↑	Extended	7	4
BB	ADDA		5	3	F1	CMPB		5	3	10FF	STS	Extended		7	4	
BC	CMPX	↓	7	3	F2	SBCB	↑			113F	SWI3	↑	Implied	20	2	
BD	JSR		8	3	F3	ADDD		7	3	1183	CMPU		Immed	5	4	
BE	LDX	↓	6	3	F4	ANDB	↑			118C	CMP5	↑	Immed	5	4	
BF	STX		Extended	6	3	F5		BITB	5	3	1193		CMPU	Direct	7	3
C0	SUBB	↑	2	2	F6	LDB	↓			119C	CMP5	↑	Direct	7	3	
C1	CMPB		2	2	F7	STB		5	3	11A3	CMPU		Indexed	7+	3+	
C2	SBCB	↓	2	2	F8	EORB	↑			11AC	CMP5	↑	Indexed	7+	3+	
C3	ADDD		4	3	F9	ADCB		5	3	11B3	CMPU		Extended	8	4	
C4	ANDB	↓	2	2	FA	ORB	↑			11BC	CMP5	↑	Extended	8	4	
C5	BITB		Immed	2	2	FB		ADDB	Extended	5	3					

Note: All unused opcodes are both undefined and illegal. The operation is not guaranteed.

Note for Use

Compatibility with NMOS MPU (HD6809)

The differences between HD6309 (CMOS) and HD6809 (NMOS) is shown in table 13.

Example: CLR (Extended)

\$8000 CLR \$A000
 \$A000 FCB \$80

Execution Sequence of CLR Instruction

Cycle-by-cycle flow of CLR instruction (direct, extended, indexed addressing mode) is shown below. In this sequence the contents of the memory location specified by the operand is read before writing 00 into it. Note that status flags, such as IRQ Flag, will be cleared by this extra data read operation when accessing the control/status register (sharing the same address between read and write) of peripheral devices.

Cycle	Address	Data	R/W	Description
1	8000	7F	1	Opcode Fetch
2	8001	A0	1	Operand Address, High Byte
3	8002	00	1	Operand Address, Low Byte
4	FFFF	*	1	VMA Cycle
5	A000	80	1	Read the Data
6	FFFF	*	1	VMA Cycle
7	A000	00	0	Store Fixed 00 into Specified Location

* The data bus has the data at that particular address.

Table 13. Differences between HD6309 and HD6809

Item		HD6309 (CMOS)	HD6809 (NMOS)
Address bus during reset operation internal transaction (Note)		Outputs FFFF ₁₆ VMA state (figure 6)	Outputs FFFE ₁₆
Memory ready (MRDY)	Stretch Unit	Integral multiples of half (1/2) bus cycles	Integral multiples of quarter (1/4) bus cycles
	Stretch Time	5 μs max	10 μs max
	Reset operation internal transaction period (Note)	VMA state E and Q are not stretched	E and Q are stretched
DMA/bus request (DMA/BREQ)	Auto-refresh	None	Executed
	External interrupt requests during DMA cycle (IRQ, FIRQ)	Not accepted (Also during dead cycle)	With auto-refresh, IRQ and FIRQ requests issued during MPU cycle are latched.
	Reset operation internal transaction period (Note)	Set DMA/BREQ to high (figure 21)	Low level DMA/BREQ allows the MPU to be placed in bus grant state (BA·BS = high).
External clock input XTAL Pin		Floating	Grounded
Unused opcode Unused Post byte code (indexed addressing, EXG and TFR instructions)		Operation is not guaranteed when unused opcode and unused post byte code are specified. Operations are different between the two devices.	

Note: Reset operation internal transaction period is a VMA period during which the address bus outputs FFFF₁₆.

Application Note for System Design

At the trailing edge of the address bus, the noise pulses may appear on the output signals in HD6309.

Note the noise pulses and the following measures against them.

Noise Occurrence Condition: As shown in figure 22, the noise pulses which are 0.8 V or over may appear on E and Q clocks when the address bus changes from high to low.

If the address buses (A_0-A_{15} , and R/\overline{W}) change from high to low, the transient current flows through the GND. The noise pulses are generated on the LSI's V_{SS} pins according

to the current and to the impedance state of the GND wirings.

Figure 23 shows the noise voltage dependency on the each parameter.

Figure 25 shows the noise voltage dependency on the load capacitance of the address bus.

Note: The noise level should be carefully checked because it depends on the each parameter of actual application system.

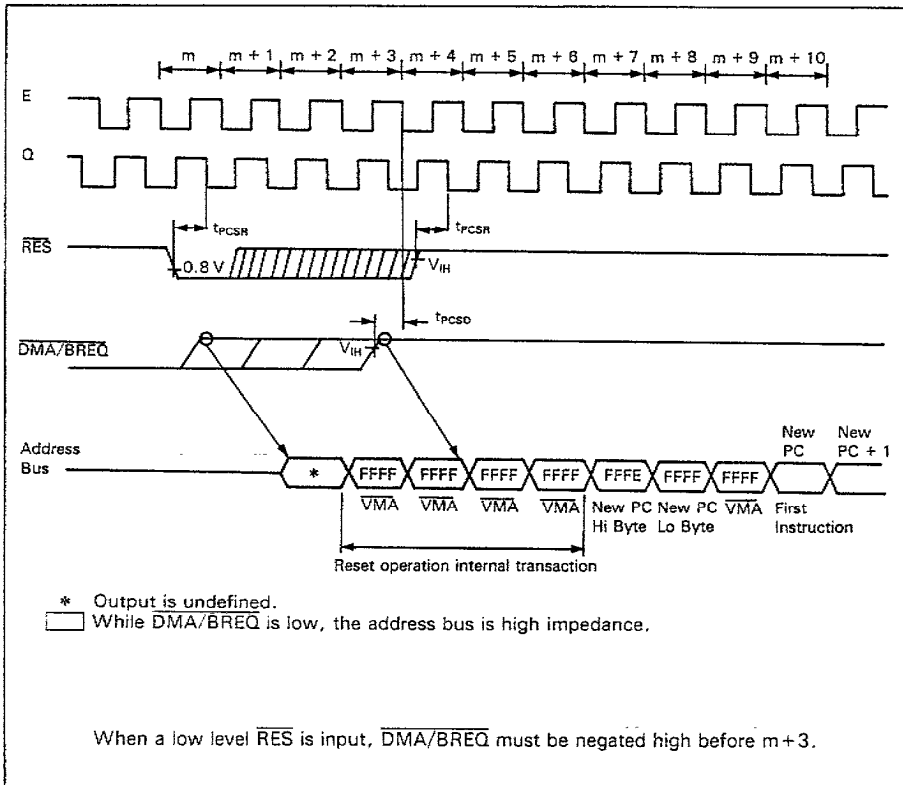


Figure 21. $\overline{DMA/BREQ}$ during reset operation internal transaction

Noise Reduction:

1. Control each parameter such as C_d , V_{CC} , Z_g in figure 23, and the noise level is reduced to be allowable.
2. Insert a bypass capacitor between the V_{CC} and the GND of the HD6309.
3. Connect the CMOS buffer with noise margin to E and Q clocks.
4. Insert the damping resistors to the address

bus. That is effective for the noise level to reduce less than 0.8 V. The damping resistor is about 40-50 Ω on the higher byte of the address bus ($A_{15}-A_8$) and about 130-140 Ω on the lower byte of the address bus (A_7-A_0), and R/\bar{W} as shown in figure 24. Electrical specifications are not changed by inserting the damping resistors.

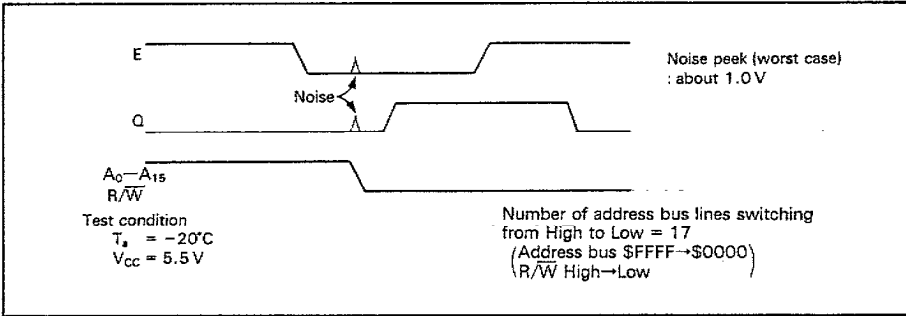


Figure 22. Noise at Address Bus Output Changing

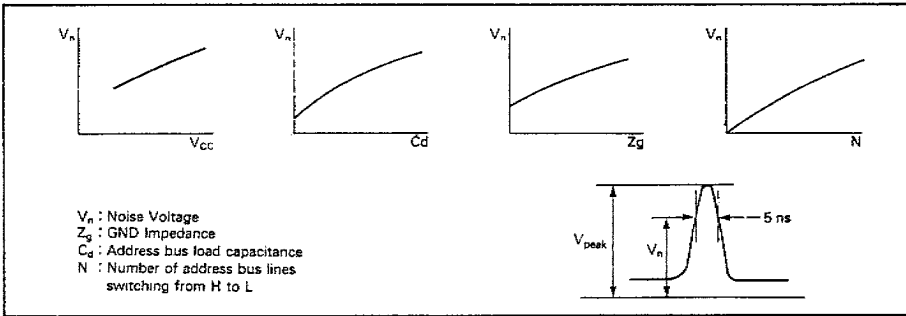


Figure 23. Dependency of the Noise Voltage on Each Parameter

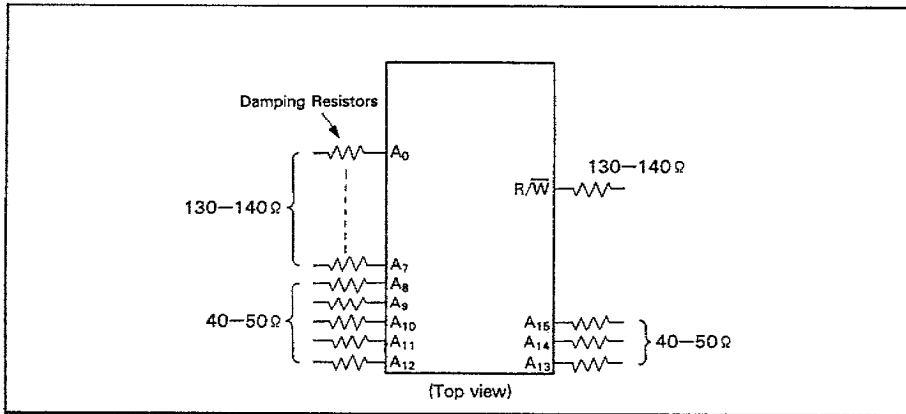


Figure 24. Connecting Damping Resistors to Address Bus

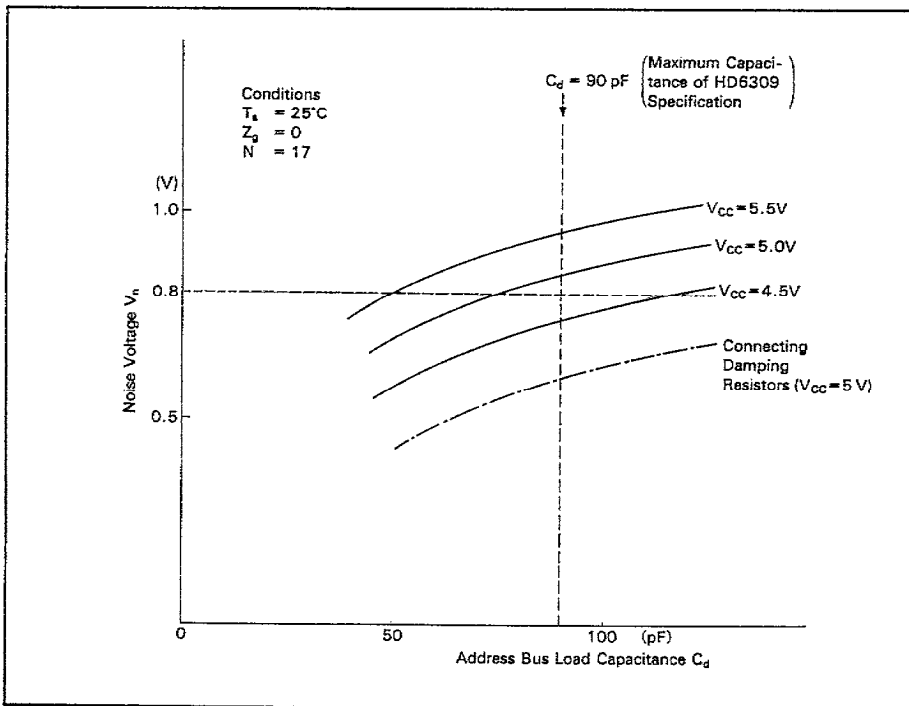


Figure 25. Dependency of the Noise Voltage on the Load Capacitance of the Address Bus

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}^1	-0.3 to +7.0	V
Input Voltage	V_{in}^1	-0.3 to +7.0	V
Maximum Output Current	$ I_o ^2$	5	mA
Maximum Total Output Current	$ \Sigma I_o ^3$	100	mA
Operating Temperature	T_{opr}	-20 to +75	°C
Storage Temperature	T_{stg}	-55 to +150	°C

- Notes: 1. With respect to V_{SS} (system GND)
 2. Maximum output current is the maximum currents which can flow out from one output terminal and I/O common terminal (A₀-A₁₅, R/W, D₀-D₇, BA, BS, Q, E).
 3. Maximum total output current is the total sum of output currents which can flow out simultaneously from output terminals and I/O common terminals (A₀-A₁₅, R/W, D₀-D₇, BA, BS, Q, E).
 4. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}^1	4.5	5.0	5.5	V
Input Voltage	EXTAL	V_{IL}^1	-0.3		0.6	V
	Other Inputs		-0.3		0.8	V
	RES	V_{IH}^1	$V_{CC}-0.5$		V_{CC}	V
	EXTAL		$V_{CC} \times 0.7$		V_{CC}	V
	Other Inputs		2.0		V_{CC}	V
Operating Temperature		T_{opr}	-20	25	75	°C

Note: 1. With respect to V_{SS} (system GND)

Electrical Characteristics

DC Characteristics ($V_{CC}=5.0\text{ V} \pm 10\%$, $V_{SS}=0\text{ V}$, $T_a=-20\text{ to }+75\text{ }^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	HD63B09			HD63C09			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Input High Voltage	RES	V_{IH}	$V_{CC}-0.5$	V_{CC}	$V_{CC}-0.5$	V_{CC}	V		
	EXTAL		$V_{CC}\times 0.7$	V_{CC}	$V_{CC}\times 0.7$	V_{CC}			
	Other Inputs		2.0	V_{CC}	2.0	V_{CC}			
Input Low Voltage	EXTAL	V_{IL}	-0.3	0.6	-0.3	0.6	V		
	Other Inputs		-0.3	0.8	-0.3	0.8			
Input Leakage Current Except EXTAL, XTAL	EXTAL, XTAL	I_{in}	-2.5	2.5	-2.5	2.5	μA	$V_{in}=0\text{ to }V_{CC}$, $V_{CC}=\text{max}$	
	Three State (Off State) D_0-D_7	I_{ISI}	-10	10	-10	10	μA	$V_{in}=0.4\text{ to }V_{CC}$, $V_{CC}=\text{max}$	
Input Current	$A_0-A_{15}, R/\bar{W}$		-10	10	-10	10		$V_{CC}=\text{max}$	
Output High Voltage	D_0-D_7	V_{OH}	4.1		4.1		V	$I_{LOAD} = -400\mu\text{A}$	
			$V_{CC}-0.1$		$V_{CC}-0.1$			$I_{LOAD} = -10\mu\text{A}$	
	$A_0-A_{15}, R/\bar{W}, Q, E$		4.1		4.1			$I_{LOAD} = -400\mu\text{A}$	
			$V_{CC}-0.1$		$V_{CC}-0.1$			$I_{LOAD} = -10\mu\text{A}$	
	BA, BS		4.1		4.1			$I_{LOAD} = -400\mu\text{A}$	
			$V_{CC}-0.1$		$V_{CC}-0.1$			$I_{LOAD} = -10\mu\text{A}$	
Output Low Voltage	V_{OL}		0.5		0.5	V	$I_{LOAD} = 2\text{mA}$		
Input Capacitance	D_0-D_7	C_{in}		15		15	pF	$V_{in}=0\text{V}$, $T_a=25^\circ\text{C}$, $f=1\text{MHz}$	
	Except D_0-D_7			10		10			
Output Capacitance	$A_0-A_{15}, R/\bar{W}, BA, BS$	C_{out}		12		12	pF		
Current Dissipation		I_{CC}		24		36	mA	Operating	
				15		18		Sleeping	

AC Characteristics ($V_{CC}=5.0\text{ V} \pm 10\%$, $V_{SS}=0\text{ V}$, $T_a=-20\text{ to }+75\text{ }^\circ\text{C}$, unless otherwise noted.)

Clock Timing

Item	Symbol	HD63B09			HD63C09			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Frequency of Operation (Crystal External Input)	f_{XTAL}	2	8	2	12		MHz	Figs. 27, 28	
Cycle Time	t_{cyc}	500		2000	333		2000	ns	
Total Up Time	t_{UT}	480			310			ns	
Processor Clock High	t_{PWEH}	220		5000	140		5000	ns	
Processor Clock Low	t_{PWEL}	210		1000	140		1000	ns	
E Rise and Fall Time	t_{Er}, t_{Ef}			20			20	ns	
E_{Low} to Q_{High} Time	t_{AVS}	100		140	70		100	ns	
Q Clock High	t_{PWQH}	220		1000	140		1000	ns	
Q Clock Low	t_{PWQL}	220		5000	140		5000	ns	
Q Rise and Fall Time	t_{Qr}, t_{Qf}			20			20	ns	
Q_{Low} to E_{Low} Time	t_{QE}	100			70			ns	

Bus Timing

Item	Symbol	HD63B09			HD63C09			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Address Delay	t_{AD}			110			110	ns	Figs. 27, 28
Address Valid to Q_{High}	t_{AQ}	15			-30			ns	
Peripheral Read Access Time ($t_{UT}-t_{AD}-t_{BSR}=t_{ACC}$)	t_{ACC}	330			160			ns	
Data Set Up Time (Read)	t_{BSR}	40			40			ns	
Input Data Hold Time	t_{DHR}	10			10			ns	
Address Hold Time	t_{AH}	$T_a=0\text{ to }+75\text{ }^\circ\text{C}$		20	$T_a=-20\text{ to }0\text{ }^\circ\text{C}$		20	ns	
Data Delay Time (Write)	t_{DWW}			110			70	ns	
Output Hold Time	t_{OHW}	$T_a=0\text{ to }+75\text{ }^\circ\text{C}$		30	$T_a=-20\text{ to }0\text{ }^\circ\text{C}$		30	ns	
				20			20		

Note: When the address bus is latched at the rising edge of Q, Q should be delayed to assure address set-up time.

Processor Control Timing

Item	Symbol	HD63B09			HD63C09			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
MRDY Set Up Time	t_{PCSM}	110		70			ns	Figs. 3 - 7	
MRDY Set Up Time 2	t_{PCSM2}	240		160			ns	Figs. 12, 13	
Interrupts Set Up Time	t_{PCS}	110		70			ns		
HALT Set Up Time	t_{PCSH}	110		70			ns		
RES Set Up Time	t_{PCSR}	110		110			ns		
DMA/BREQ Set Up Time	t_{PCSD}	110		70			ns		
Processor Control Rise and Fall Time	t_{PCr} t_{PCf}			100			100 ns		
Crystal Oscillator Start Time	t_{ac}	20		20			ms		

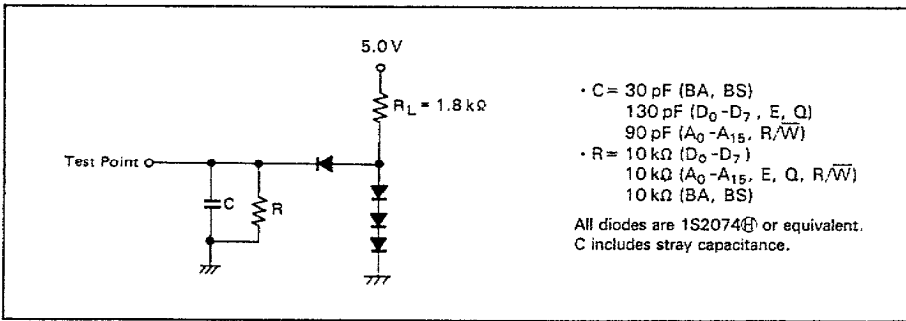


Figure 26. Bus Timing Test Load

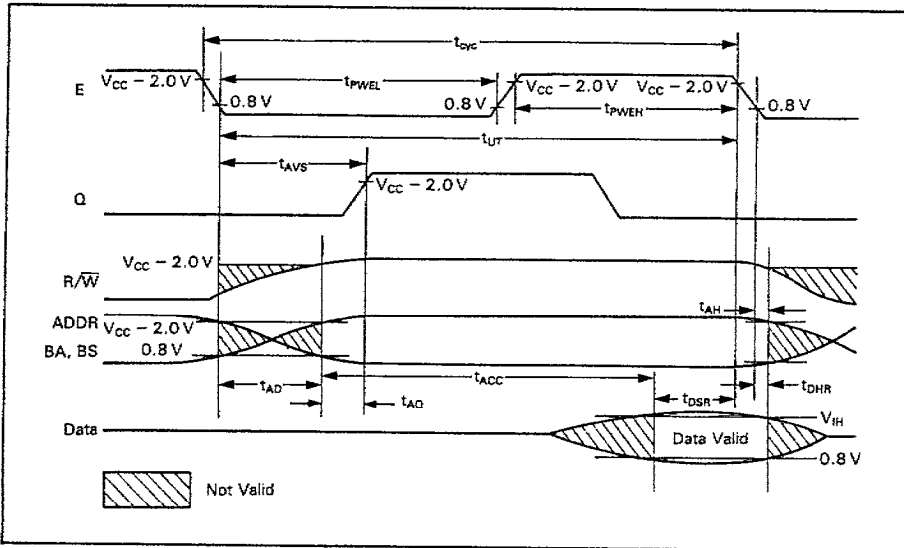


Figure 27. Read Data from Memory or Peripherals

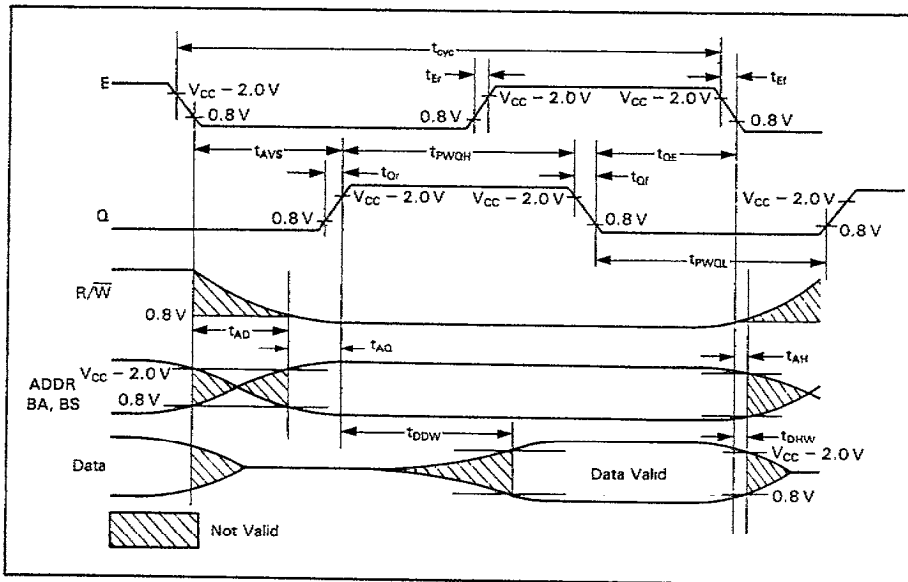


Figure 28. Write Data to Memory or Peripherals

Package Dimensions

Unit:mm (inch)

