

## SNx4LS245 Octal Bus Transceivers With 3-State Outputs

### 1 Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

### 2 Applications

- Building Automation
- Electronic Point of Sale
- Factory Automation and Control
- Test and Measurement

### 3 Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

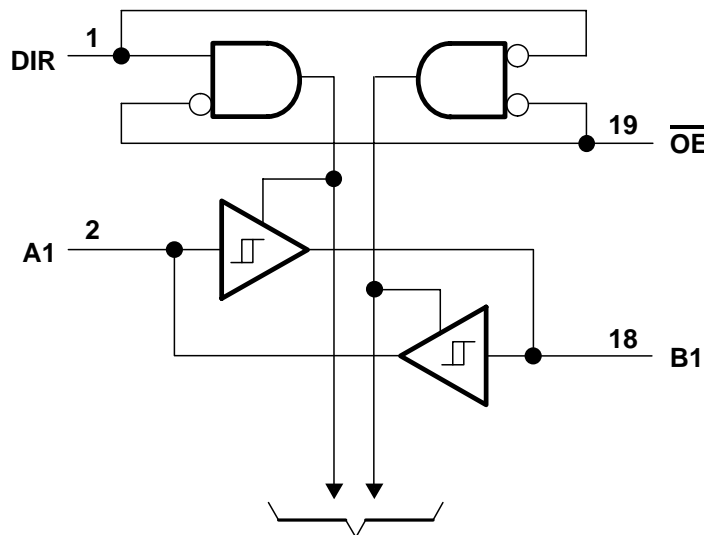
The SNx4LS245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can disable the device so that the buses are effectively isolated.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54LS245J	CDIP (20)	24.20 mm x 6.92 mm
SN54LS245W	CFP (20)	7.02 mm x 13.72 mm
SN54LS245FK	LCCC (20)	8.89 mm x 8.89 mm
SN74LS245DB	SSOP (20)	7.20 mm x 5.30 mm
SN74LS245DW	SOIC (20)	12.80 mm x 7.50 mm
SN74LS245N	PDIP (20)	24.33 mm x 6.35 mm
SN74LS245NS	SO (20)	12.60 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



#### To Seven Other Channels

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

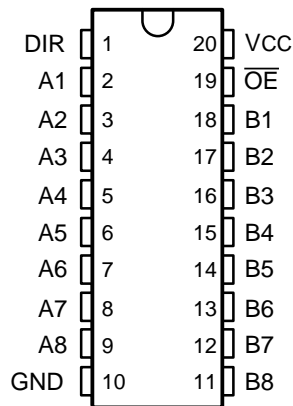
<b>Changes from Revision A (February 2002) to Revision B</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet .....	<b>1</b>
• Changed $R_{\theta JA}$ values in <i>Thermal Information</i> table: 70 to 91.7 for DB package, 58 to 79 for DW package, 69 to 46.1 for N package, and 60 to 74.2 for NS package .....	<b>4</b>

## 5 Device Comparison Table

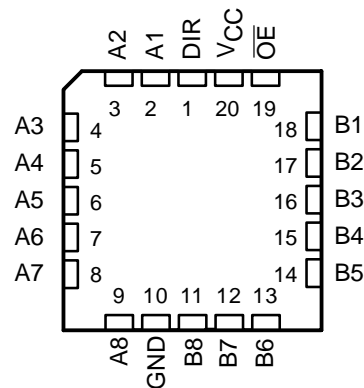
TYPE	$I_{OL}$ (SINK CURRENT)	$I_{OH}$ (SOURCE CURRENT)
SN54LS245	12 mA	-12 mA
SN74LS245	24 mA	-15 mA

## 6 Pin Configuration and Functions

J, W, DB, DW, N, or NS Package  
20-Pin CDIP, CFP, SSOP, SOIC, PDIP, or SO  
Top View



FK Package  
20-Pin LCCC  
Top View



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	I	Controls signal direction; Low = Bx to Ax, High = Ax to Bx
2	A1	I/O	Channel 1, A side
3	A2	I/O	Channel 2, A side
4	A3	I/O	Channel 3, A side
5	A4	I/O	Channel 4, A side
6	A5	I/O	Channel 5, A side
7	A6	I/O	Channel 6, A side
8	A7	I/O	Channel 7, A side
9	A8	I/O	Channel 8, A side
10	GND	—	Ground
11	B8	O/I	Channel 8, B side
12	B7	O/I	Channel 7, B side
13	B6	O/I	Channel 6, B side
14	B5	O/I	Channel 5, B side
15	B4	O/I	Channel 4, B side
16	B3	O/I	Channel 3, B side
17	B2	O/I	Channel 2, B side
18	B1	O/I	Channel 1, B side
19	$\overline{OE}$	I	Active low output enable; Low = all channels active, High = all channels disabled (high impedance)
20	V <sub>CC</sub>	—	Power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage		7	V
$V_I$	Input voltage <sup>(1)</sup>		7	V
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

(1) All voltage values are with respect to GND.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	SN54LS245	4.5	5	5.5	V
		SN74LS245	4.75	5	5.25	
$I_{OH}$	High-level output current	SN54LS245			-12	mA
		SN74LS245			-15	
$I_{OL}$	Low-level output current	SN54LS245			12	mA
		SN74LS245			24	
$T_A$	Operating free-air temperature	SN54LS245	-55		125	°C
		SN74LS245	0		70	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SNx4LS245							UNIT	
	J (CDIP)	W (CFP)	FK (LCCC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)		
	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	N/A	N/A	91.7	79.0	46.1	74.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3 <sup>(2)</sup>	70.1 <sup>(2)</sup>	46.7 <sup>(2)</sup>	53.1	44.4	32.1	40.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9 <sup>(2)</sup>	109.5 <sup>(2)</sup>	45.6 <sup>(2)</sup>	46.8	46.9	27.0	41.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	N/A	N/A	N/A	18.9	18.0	17.6	16.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	N/A	N/A	N/A	46.4	46.3	26.9	41.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.9 <sup>(2)</sup>	13.0 <sup>(2)</sup>	6.7 <sup>(2)</sup>	N/A	N/A	N/A	N/A	°C/W

 (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

 (2) MIL-STD-883 for  $R_{th-JC}$  JEDEC JESD51 for  $R_{th-JB}$  (body not contact PCB)

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IH</sub>	High-level input voltage			2			V
V <sub>IL</sub>	Low-level input voltage	SN54LS245				0.7	V
		SN74LS245				0.8	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5	V
Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		A or B	V <sub>CC</sub> = MIN	0.2	0.4		V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL(max)</sub> V <sub>IH</sub> = 2 V,	I <sub>OH</sub> = -3 mA	2.4	3.4		V
			I <sub>OH</sub> = MAX	2			
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL(max)</sub>	I <sub>OL</sub> = 12 mA			0.4	V
			I <sub>OL</sub> = 24 mA	SN74LS245			
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, OE at 2 V	V <sub>O</sub> = 2.7 V			20	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, OE at 2 V	V <sub>O</sub> = 0.4 V			-200	μA
I <sub>I</sub>	Input current at maximum input voltage	A or B DIR or OE	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5 V		0.1	mA
				V <sub>I</sub> = 7 V		0.1	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2.7 V			20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>IL</sub> = 0.4 V			-0.2	mA
I <sub>OS</sub>	Short-circuit output current <sup>(2)</sup>	V <sub>CC</sub> = MAX		-40		-225	mA
I <sub>CC</sub>	Supply current	Total, outputs high	V <sub>CC</sub> = MAX Outputs open		48	70	mA
		Total, outputs low			62	90	
		Outputs at high Z			64	95	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

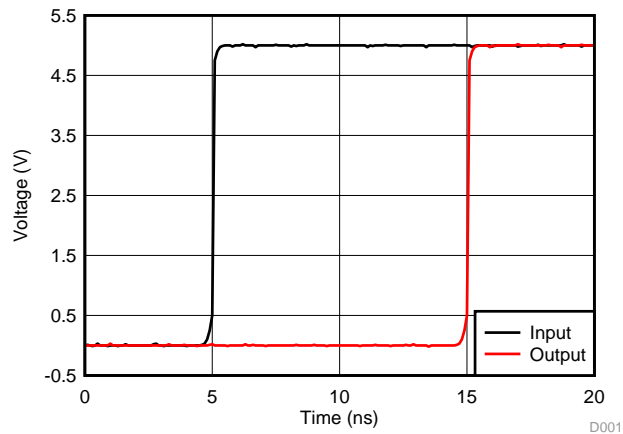
(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## 7.6 Switching Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 2)

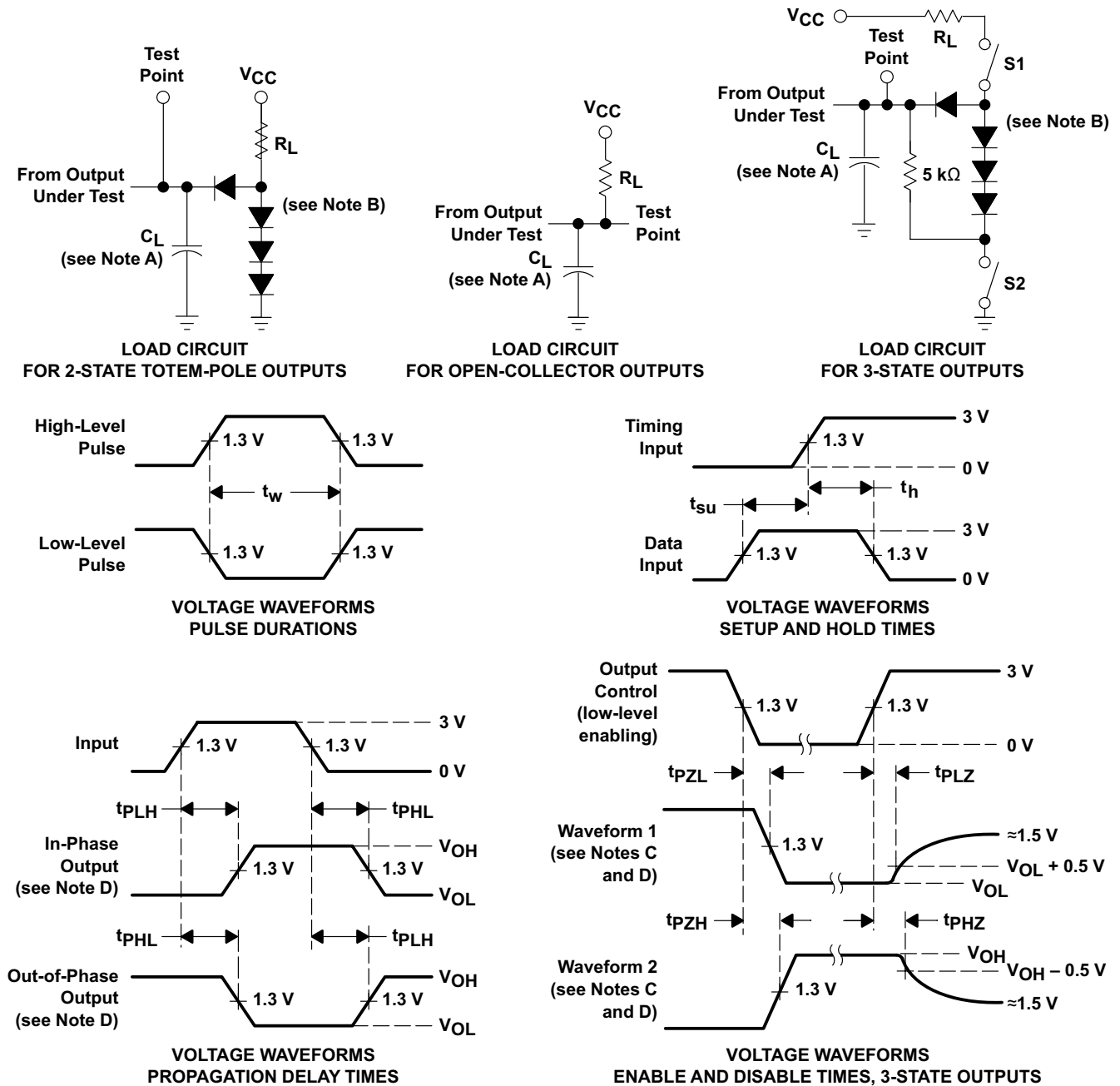
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω		8	12	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output			8	12	
t <sub>PZL</sub>	Output enable time to low level	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω		27	40	ns
t <sub>PZH</sub>	Output enable time to high level			25	40	
t <sub>PLZ</sub>	Output disable time from low level	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 667 Ω		15	25	ns
t <sub>PHZ</sub>	Output disable time from high level			15	28	

## 7.7 Typical Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 45\text{ pF}$ ,  $R_L = 667\ \Omega$ 


**Figure 1. Simulated Propagation Delay From Input to Output**

## 8 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{pZH}$ ; S1 is closed and S2 is open for  $t_{pZL}$ .  
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
 F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.  
 G. The outputs are measured one at a time with one input transition per measurement.

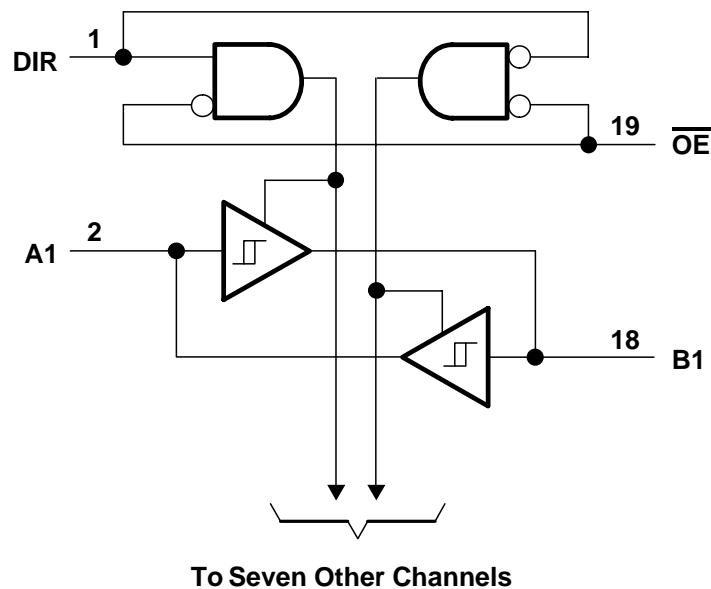
Figure 2. Load Circuits and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

The SNx4LS245 uses Schottky transistor logic to perform the standard '245 transceiver function. This standard logic function has a common pinout, direction select pin, and active-low output enable. When the outputs are disabled, the A and B sides of the device are effectively isolated.

### 9.2 Functional Block Diagram



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**Figure 3. Logic Diagram (Positive Logic)**

### 9.3 Feature Description

#### 9.3.1 3-State outputs

The 3-state outputs can drive bus lines directly. All outputs can be put into high impedance mode through the  $\overline{OE}$  pin.

#### 9.3.2 PNP Inputs

This device has PNP inputs which reduce dc loading on bus lines.

#### 9.3.3 Hysteresis on Bus Inputs

The bus inputs have built-in hysteresis that improves noise margins.

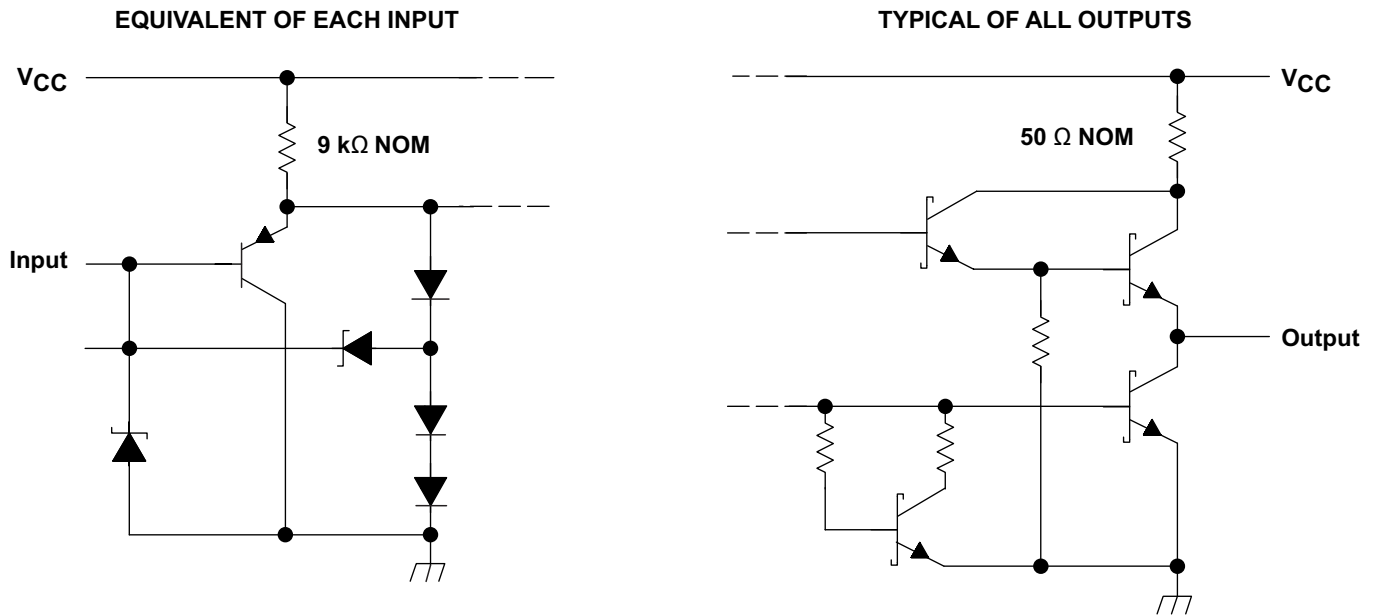
### 9.4 Device Functional Modes

The SNx4LS245 performs the standard '245 logic function. Data can be transmitted from A to B or from B to A depending on the DIR pin value, or the A and B sides can be isolated from one another by setting the  $\overline{OE}$  pin HIGH.



**Table 1. Function Table**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



**Figure 4. Schematics of Inputs and Outputs**

## 10 Application and Implementation

### NOTE

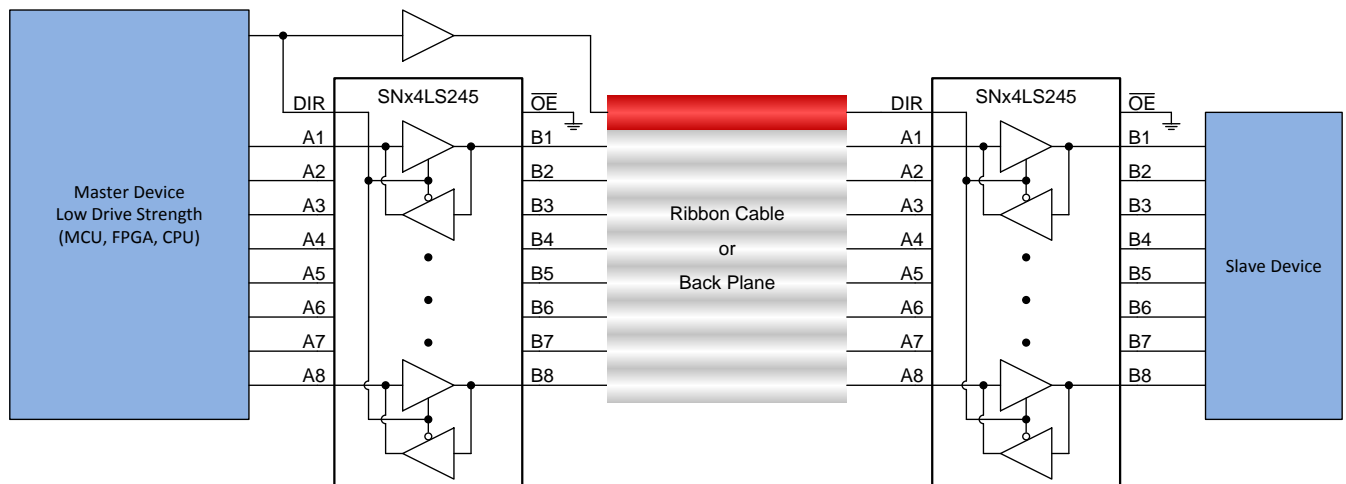
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SNx4LS245 is commonly used to drive ribbon cables or back plane busses. It allows isolation from the bus when necessary, and increases drive strength on the bus.

### 10.2 Typical Application

Figure 5 shows the SNx4LS245 wired up as a permanently enabled data bus transceiver for both a master and slave device communicating over a ribbon cable or back plane.



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**Figure 5. SNx4LS245 Being Used to Communicate Over a Ribbon Cable or Back Plane**

#### 10.2.1 Design Requirements

This device uses Schottky transistor logic technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

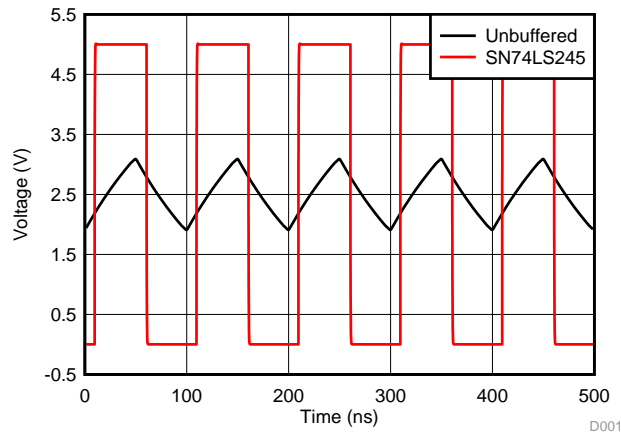
#### 10.2.2 Detailed Design Procedure

- Power Supply
  - Each device must maintain a supply voltage between 4.5 V and 5.5 V
- Inputs
  - Input signals must meet the  $V_{IH}$  and  $V_{IL}$  specifications in [Electrical Characteristics](#)
  - Inputs leakage values ( $I_I$ ,  $I_{IH}$ ,  $I_{IL}$ ) from [Electrical Characteristics](#) must be considered
- Outputs
  - Output signals are specified to meet the  $V_{OH}$  and  $V_{OL}$  specifications in [Electrical Characteristics](#) as a minimum (the values could be closer to  $V_{CC}$  for high signals or GND for low signals)
  - TI recommends maintaining output currents as specified in [Recommended Operating Conditions](#)
  - The part can be damaged by sourcing or sinking too much current. See [Electrical Characteristics](#) for details.

## Typical Application (continued)

### 10.2.3 Application Curve

It is common to see significant losses in ribbon cables and back planes. Figure 6 shows a simplified simulation of a ribbon cable from a 5-V, 10-MHz low-drive strength source. It shows the difference between an input signal from a weak driver like an MCU or FPGA compared to a strong driver like the SN74LS245 when measured at the distant end of the cable. By adding a high-current drive transceiver before the cable, the signal strength can be significantly improved, and subsequently the cable can be longer.



Unbuffered line is directly connected to low current source, SN74LS245 line is buffered through the transceiver. Both signals are measured at the distant end of the ribbon cable. **Input signal is not shown.**

**Figure 6. Simulated Outputs From Ribbon Cable With a 5-V, 10-MHz Source**

## 11 Power Supply Recommendations

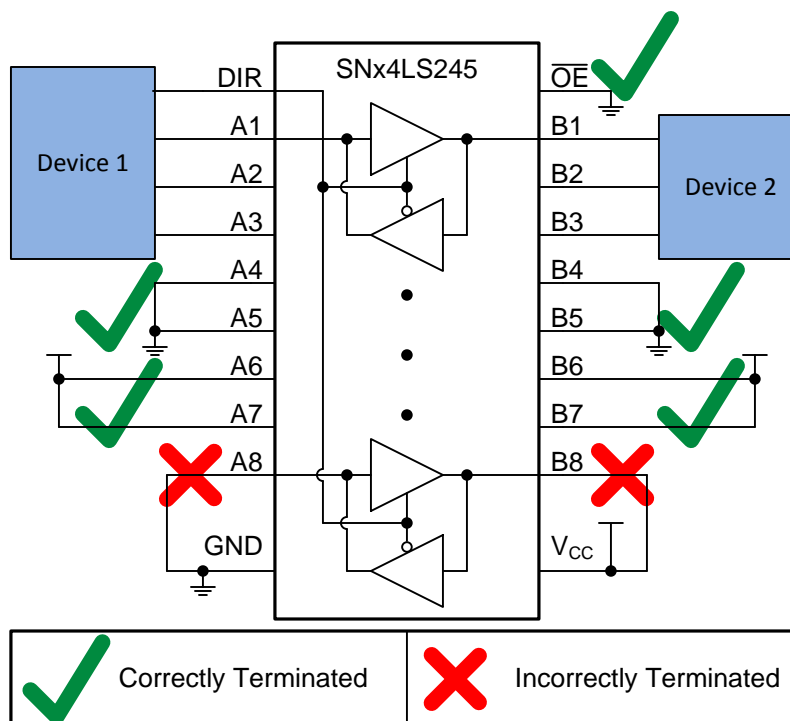
The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#). Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu\text{F}$  bypass capacitor. If there are multiple  $V_{CC}$  pins, TI recommends a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices, inputs must not be left floating. In many applications, some channels of the SNx4LS245 are unused, and thus must be properly terminated. Because each transceiver channel pin can be either an input or an output, they must be treated as both when being terminated. Ground or  $V_{CC}$  (whichever is more convenient) can be used to terminate unused inputs; however, each unused channel should be terminated to the same logic level on both the A and B side. For example, in [Figure 7](#) unused channels 4, 5, 6, and 7 are terminated correctly with both sides connected to the same voltage, while channel 8 is terminated incorrectly with each side being tied to a different voltage. The  $\overline{\text{OE}}$  input is also unused in this example, and is terminated directly to ground to permanently enable all outputs.

### 12.2 Layout Example



**Figure 7. Example Demonstrating How to Terminate Unused Inputs and Channels of a Transceiver**

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LS245	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LS245	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8002101VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8002101VS A SNV54LS245W	<a href="#">Samples</a>
80021012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	80021012A SNJ54LS 245FK	<a href="#">Samples</a>
8002101SA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8002101SA SNJ54LS245W	<a href="#">Samples</a>
JM38510/32803B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32803B2A	<a href="#">Samples</a>
JM38510/32803BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32803BRA	<a href="#">Samples</a>
JM38510/32803BSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32803BSA	<a href="#">Samples</a>
M38510/32803B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32803B2A	<a href="#">Samples</a>
M38510/32803BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32803BRA	<a href="#">Samples</a>
M38510/32803BSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32803BSA	<a href="#">Samples</a>
SN54LS245J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS245J	<a href="#">Samples</a>
SN74LS245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	<a href="#">Samples</a>
SN74LS245DW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	
SN74LS245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS245	<a href="#">Samples</a>
SN74LS245N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS245N	<a href="#">Samples</a>
SN74LS245NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS245N	<a href="#">Samples</a>
SN74LS245NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS245	<a href="#">Samples</a>
SNJ54LS245FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	80021012A SNJ54LS	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										245FK	
SNJ54LS245J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS245J	<a href="#">Samples</a>
SNJ54LS245W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8002101SA SNJ54LS245W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS245, SN54LS245-SP, SN74LS245 :**

- Catalog : [SN74LS245](#), [SN54LS245](#)
- Military : [SN54LS245](#)
- Space : [SN54LS245-SP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS245DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LS245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS245NSR	SO	NS	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8002101VSA	W	CFP	20	25	506.98	26.16	6220	NA
80021012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8002101SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/32803B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/32803BSA	W	CFP	20	25	506.98	26.16	6220	NA
M38510/32803B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/32803BSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LS245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS245NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS245FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS245W	W	CFP	20	25	506.98	26.16	6220	NA

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

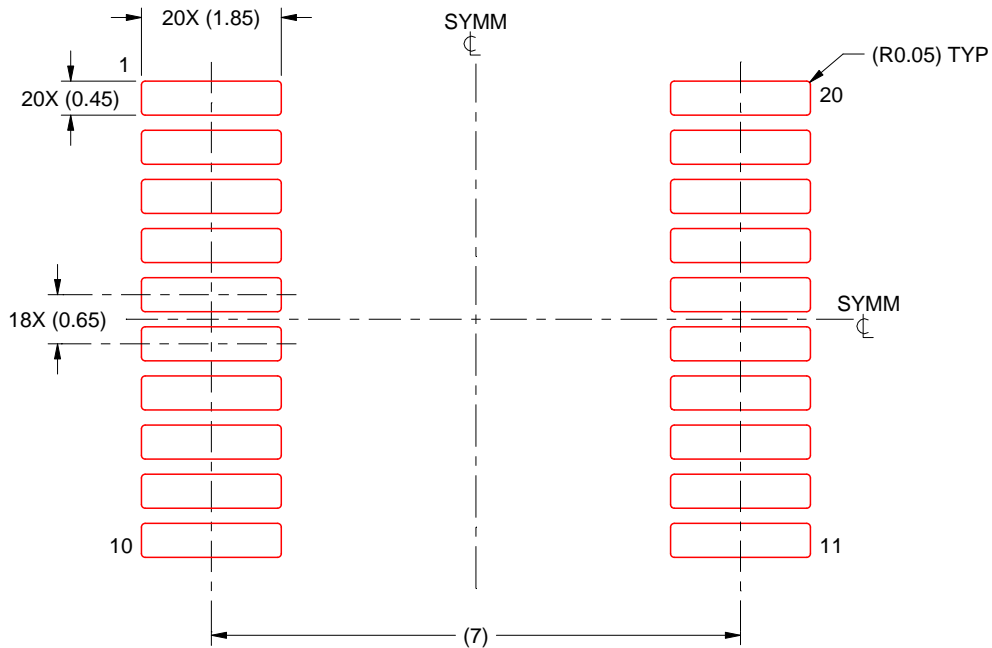
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

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