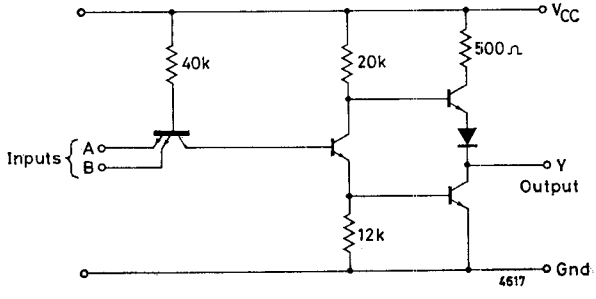
SERIES 54L00/74L00

The 54L00/74L00 range of low-power transistor-transistor logic circuits featured here are more comprehensively described in – Low Power TTL: A Ferranti publication – List No. ESB 63



Equivalent Basic Function

FEATURES

- Very low-power dissipation – typically 1 mW per gate at 50% duty cycle
- Relatively high speed – typical gate propagation delay time of 33 ns
- High noise immunity – typically 1V at $T_{amb} = 25°C$
- Low output impedance in both states
- High fan-out – maximum 10
- Compatible with most other logic families – supply voltage 5V
- Choice of ceramic or moulded D.I.L. package

	Typical Propagation Delay	Temperature Range	Package
Series 54L00			
Series 54L00E	33 ns	–55 to +125°C	Moulded Dual in-Line
Series 54L00J	33 ns	–55 to +125°C	Ceramic Dual in-Line
Series 64L00			
Series 64L00E	33 ns	–40 to +85°C	Moulded Dual in-Line
Series 64L00J	33 ns	–40 to +85°C	Ceramic Dual in-Line
Series 74L00			
Series 74L00E	33 ns	0 to +70°C	Moulded Dual in-Line
Series 74L00J	33 ns	0 to +70°C	Ceramic Dual in-Line