TC5091AP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5091AP PENTAPHASIC INTEGRATION 8-BIT A/D CONVERTER

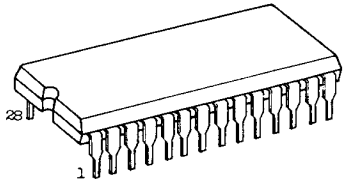
The TC5091AP is a pentaphasic integration 8-bit A/D converter of high precision and low power consumption. The 8-bit output data can be taken out in the form of time-shared higher order 4 bits and lower order 4 bits on four 3-state data output. Either the higher order bits or the lower order bits can be selected by RSEL input. This output system is designed specifically considering interface to 4-bit CPU.
Further, since this converter has an analog multiplexer capable of selecting the input data up to six channels, an over-range flag, and a serial clock output function, it is used for a variety of applications.

FEATURES:

- High precision : ±LSB(Max.)
- Low power consumption: 10mW(Typ.) @(V_{DD}=5V, f_{OSC}=1MHz)
- Single power supply : V_{DD}=5±1.5V
- High-speed conversion: 2ms(Max.) @f_{OSC}=1.5MHz
- 6-channel analog multiplexer contained
- Reference clock oscillation cirucit contained (CR oscillation)
- 3-state output with output latch
- TTL/CMOS compatible digital Input/Output
- Offset automatic correction

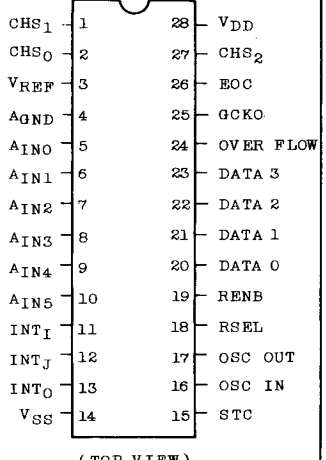
APPLICATIONS:

- Various control instruments (for temperature, humidity, pressure, etc.)
- Home electric appliances
- Electrical wiring apparatuses
- Battery-driven instruments



DIP 28 (6D28A-P)

PIN ASSIGNMENT

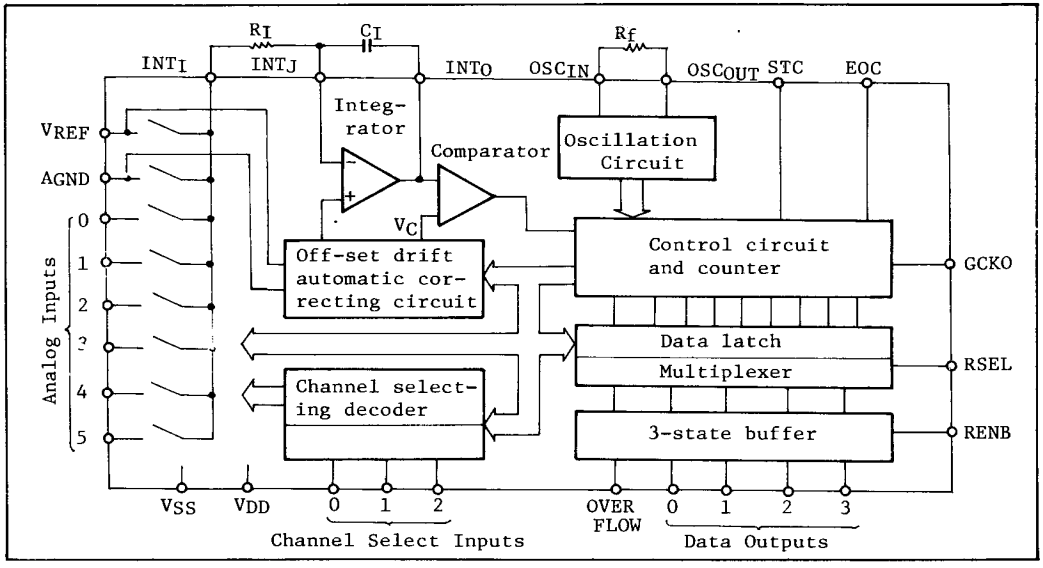


(TOP VIEW)

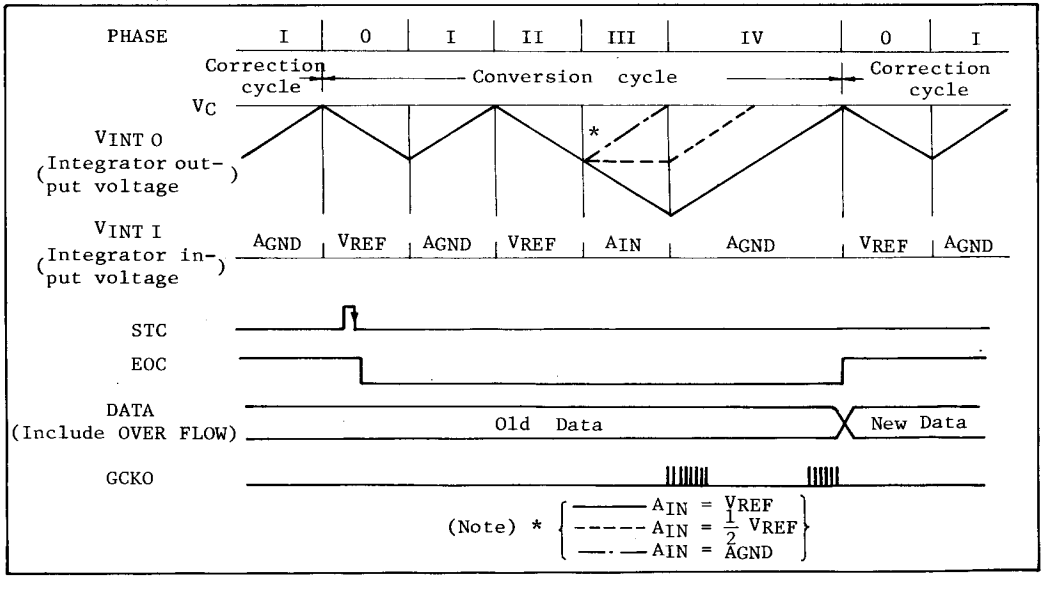
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+8	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Reference Supply Voltage	V_{REF}	V_{AGND} ~ V_{DD}+0.5	V
Analog Ground Voltage	V_{AGND}	V_{SS}-0.5 ~ V_{REF}	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

BLOCK DIAGRAM



TIMING DIAGRAM



FUNCTION OF EACH PIN

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>NAME & FUNCTION</th><th>PIN No.</th><th>SYMBOL</th><th>NAME & FUNCTION</th></tr>
<tr><td>1</td><td>CHS 1</td><td>(Channel Select Inputs)
Address inputs to select analog inputs, which consist of three terminals of CHS0∿2.
These select inputs are taken into the internal latch by the falling edge of STC inputs.
Test mode should not be used.</td><td>16</td><td>OSC IN</td><td rowspan="2">I/O for reference clocl oscillation. Clock oscillation can be made by means of external registance. Clock can be supplied from outside through input of OSC IN.</td></tr>
<tr><td>2</td><td>CHS 0</td><td>TRUTH TABLE OF MULTIPLEXER
<table><tr><th>CHS2</th><th>CHS1</th><th>CHS0</th><th>ON channel</th></tr><tr><td>L</td><td>L</td><td>L</td><td>VREF*</td></tr><tr><td>L</td><td>L</td><td>H</td><td>AGND*</td></tr><tr><td>L</td><td>H</td><td>L</td><td>AIN0</td></tr><tr><td>L</td><td>H</td><td>H</td><td>AIN1</td></tr><tr><td>H</td><td>L</td><td>L</td><td>AIN2</td></tr><tr><td>H</td><td>L</td><td>H</td><td>AIN3</td></tr><tr><td>H</td><td>H</td><td>L</td><td>AIN4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>AIN5</td></tr></table>* Test Conditions</td><td>17</td><td>OSC OUT</td></tr>
<tr><td>3</td><td>VREF</td><td>(Reference Voltage)
Reference voltage supplying terminal, which performs as full-scale voltage of AIN.</td><td>18</td><td>RSEL</td><td>(Read Select)
Input to select the higher order 4 bits or the lower order 4 bits to 4-bit data output.
"H": Output of the higher order 4 bits.
"L": Output of the lower order 4 bits.</td></tr>
<tr><td>4</td><td>AGND</td><td>(Analog Ground)
Electrical potential to determine "zero point" of AIN.</td><td>19</td><td>RENB</td><td>(Read Enable)
Data read signal.
"H": The data 0∿3 and overflow can be output.
"L": The output above is at high impedance.</td></tr>
<tr><td>5</td><td>AIN 0</td><td rowspan="6">(Analog Input)
Analog input terminals, by which AIN selected by CHS inputs are integrated. Input voltage range is AGND∿VREF.</td><td>20</td><td>DATA 0</td><td rowspan="4">(3-state Parallel Data Outputs)
Conversion data output.
The data 0 is LSB, and the data 3 is MSB.</td></tr>
<tr><td>6</td><td>AIN 1</td><td>21</td><td>DATA 1</td></tr>
<tr><td>7</td><td>AIN 2</td><td>22</td><td>DATA 2</td></tr>
<tr><td>8</td><td>AIN 3</td><td>23</td><td>DATA 3</td></tr>
<tr><td>9</td><td>AIN 4</td><td rowspan="2">24</td><td rowspan="2">OVER-FLOW</td><td rowspan="2">In case of overrange or underranbe, "H" level is output and the output is 3-state output.</td></tr>
<tr><td>10</td><td>AIN 5</td></tr>
<tr><td>11</td><td>INT I</td><td rowspan="3">(Integrator Input, Integrator Junction, Integrator Output)
Integrator consists of external resistor RI and external capacitor CI.</td><td rowspan="2">25</td><td rowspan="2">GCKO</td><td rowspan="2">(Gated Clock Output)
Pulses of number equivalent to the conversion data are output during conversion
(356 pulses at full scale)</td></tr>
<tr><td>12</td><td>INT J</td></tr>
<tr><td>13</td><td>INT O</td><td rowspan="2">26</td><td rowspan="2">EOC</td><td rowspan="2">(End of Conversion)
Conversion endig signal. EOC goes to "L" level at the fall of STC, and returns to "H" level at the end of conversion.</td></tr>
<tr><td>14</td><td>VSS</td><td>(Digital Ground)
Normally 0V</td></tr>
<tr><td>15</td><td>STC</td><td>(Start Conversion)
Conversion starting signal. Conversion starts at the falling edge.</td><td>27</td><td>CHS 2</td><td>(Channel Select Input)
Refer to Pins 1 and 2.</td></tr>
<tr><td></td><td></td><td></td><td>28</td><td>VDD</td><td>(Power Supply)
5V ± 1.5V</td></tr>
</table>

FUNCTIONAL DESCRIPTION

(1) System Description (Pentaphasic Integration)

The operation of the TC5091AP is composed of the correction cycle and the conversion cycle as shown in the timing chart. While the power is switched on, the repetition of correction cycle and conversion cycle enables the TC5091AP at make A/D conversion under the optimum conditions at all times. The operation flowcahrt is shown in Fig. 1.

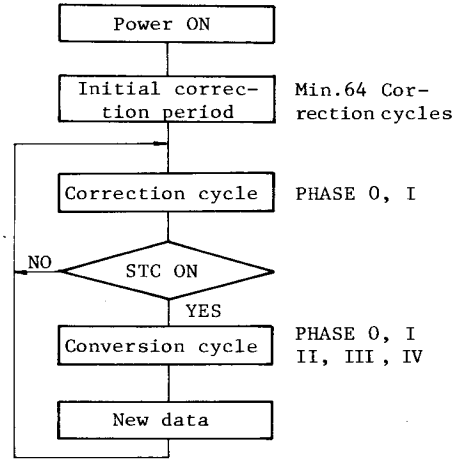


Fig. 1 Operation Flowchart

(a) Initial correction period

The internal state of this LSI is reasonably unsettled at the time when the power is switched on; therefore, the initial correction cycle is requires before stable coverting operation becomes possible.

The correction cycle automatically corrects conversion error caused by offset voltage of the integrator or the like, and is composed of the period (PHASE 0) for which V_{REF} is integrated and the period (PHASE I) for which AGND is integrated.

Since system correction is performed in steps at the end of this PHASE I, 64 correction cycles ($64 \times 1024 \cdot T_{OSC}$) are required as the initial correction period. (T_{OSC} denotes one clock cycle.)

(b) Conversion cycle

If the initial correction cycle period is completed, normal conversion becomes possible.

When STC input is given, (although the correction cycle in PHASE 0 or PHASE I is in operation at this time), the correction operation stops, and the conversion cycle starts.

In other words, even if STC input is given, this LSI performs the same operation as the correction cycle until PHASE I is completed; but it does not perform the correction at the time of completion of PHASE I, and shifts to PHASE II. Therefore, attention should be given to the fact that PHASE I prior to PHASE II does not act as correction cycle.

When STC input is given, the LSI integrates analog input in PHASE III through PHASE I and PHASE II, performing digital conversion in PHASE IV. When the LSI completes digital conversion in PHASE IV, the output is turned to the new data and the LSI returns to the correction cycle.

(c) Correction cycle

When the next STC input is given between completion of arbitrary conversion cycle (at the time of completion of PHASE IV) and completion of one correction cycle ($1024 \cdot T_{OSC}$), no correction is substantially made. Therefore, in case the STC input is consecutively given, another STC should be given after the lapse of one correction cycle at the earliest from completion of PHASE IV. When the STC input is given during conversion (While EOC is at "L" level), the STC cannot be accepted.

(d) Constant of integration

The R_I and C_I composing the integrator should be selected to satisfy the following equation.

$$R_I C_I = (0.9 \sim 2.5) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{OSC}} \text{ [S]}$$

Attention should be paid to the fact that, when the external R oscillation is used, f_{OSC} has ±30% variations in regard to the typ. value in Fig. 5 due to variations in sample and temperature characteristic.

In other words, if the typ. value in Fig. 5 is denoted by $f_{R \cdot TYP}$, the R_I and C_I should be selected according to the following equation.

$$R_I C_I = (1.2 \sim 1.75) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{R \cdot TYP}} \text{ [S]}$$

(2) Output Data Mode

TRUTH TABLE

RENB	ANALOG INPUT	DIGITAL OUTPUTS								OVER FLOW
		RSEL = "L"				RSEL = "H"				
		DATA 0	DATA 1	DATA 2	DATA 3	DATA 0	DATA 1	DATA 2	DATA 3	
L	Don't Care	High Impedance								
H	$\sim \frac{1}{2}$LSB	L	L	L	L	L	L	L	H	H
H	$\frac{1}{2}$LSB $\sim \frac{1}{2}$LSB	L	L	L	L	L	L	L	L	L
H	$\frac{1}{2}$LSB $\sim \frac{3}{2}$LSB	H	L	L	L	L	L	L	L	L
H	.....	Straight Binary								
H	"FS"-$\frac{5}{2}$LSB ~ "FS"-$\frac{3}{2}$LSB	L	H	H	H	H	H	H	H	L
H	"FS"-$\frac{3}{2}$LSB ~ "FS"-$\frac{1}{2}$LSB	H	H	H	H	H	H	H	H	L
H	"FS"-$\frac{1}{2}$LSB ~	H	H	H	H	H	H	H	H	H

Note : • AGND = 0V • 1LSB = "FS"/256

• "FS" ..... Full Scale (=V_{REF})

8-bit digital data is output on four data lines after having been divided into the higher order 4 bits and the lower order 4 bits. Either the higher order bits or the lower order bits can be selected by RSEL.

(3) System Clock Oscillation Circuit

For oscillating reference clock the oscillation circuit is composed of external resistors as shown in Fig. 2.

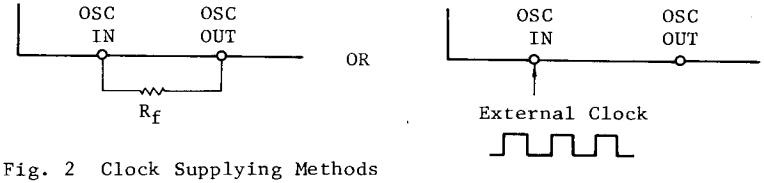


Fig. 2 Clock Supplying Methods

(4) Timings for STC-EOC and EOC-DATA

o Time (t_{SE}) from the fall of STC to the fall of EOC.

$$t_{SE} = \frac{1}{2} T_{OSC} \sim \frac{3}{2} T_{OSC}$$

o Time (t_{DE}) from the out of DATA output to the rise of EOC

$$t_{DE} = \frac{1}{2} T_{OSC}$$

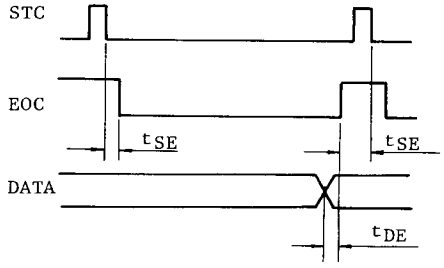


Fig. 3 Timing Chart of STC, EOC

O Min. time (t_{ES}) from the rise of EOC to the acceptance of another STC.

$$t_{ES} = \frac{1}{2} T_{OSC} \sim \frac{3}{2} T_{OSC}$$

(5) GCKO Output (Gated Clock Output)

During the conversion (PHASE IV), the pulses of number equivalent to the values of digital data can be obtained on GCKO output.
The output pluse has the frequency corresponding to four times of refernece clock as shown in Fig. 4, and is synchronized with the rising edge of OSC OUT.

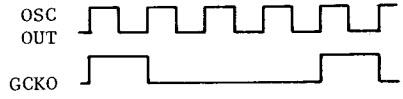


Fig. 4 Timing Chart of GCKO Output

(6) Timing for STC Input and CHS Input

STC signal is taken in synchronously with the internal clock.
Therefore, if T_{OSC} denotes one clock cycle of OSC terminal, the pulse width of more than $(2 \cdot T_{OSC})$ is required.
Since the data of $CHS_{0 \sim 2}$ are also latched in synchronously with the internal clock, the CHS signal at least requires the hold time of $(T_{OSC} + 50ns)$ or more after the fall of STC.

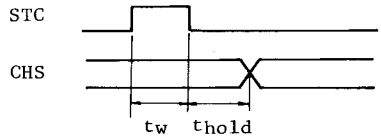


Fig.5 Timing Chart of Control Input

NOTE : $t_w > 2 \cdot T_{OSC}$, $t_{hold} > T_{OSC} + 50ns$

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

ITEM	SYMBOL		MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		3.5	5	6.5	V
Input Voltage	V_{IN}		0	–	V_{DD}	V
Reference Voltage	V_{REF}		3	–	V_{DD}	V
Analog Ground Voltage	V_{AGND}		0	0	1	V
Integral Resistor	R_I		0.4	–	2	MΩ
Integral Capacitor	C_I	(Note)	–	–	–	–
Oscillatory Resistance	R_f	V_{DD} = 5V	10	–	–	MΩ

Note: Refer to the operating consideration (1) for determing the values of R_I and C_I respectively.
The ripples of V_{DD} and V_{REF} should be held down to less than 1/256 of the respective absolute values in view of precision.

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

ITEM	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Output High Voltage	V_{OH}	$\|I_{OUT}\|$ <1 μA V_{IN}=V_{SS},V_{DD}	5	4.95	–	4.95	5.00	–	4.95	–	V
Output Low Voltage	V_{OL}	$\|I_{OUT}\|$ <1 μA V_{IN}=V_{SS},V_{DD}	5	–	0.05	–	0.00	0.05	–	0.05	V
Output High Current	I_{OH}	V_{OH}=4.0V V_{IN}=V_{SS},V_{DD} *	5	-1.2	–	-1.0	-2.0	–	-0.7	–	mA
Output Low Current	I_{OL}	V_{OL}=0.4V V_{IN}=V_{SS},V_{DD} *	5	2.4	–	2.0	4.0	–	1.6	–	mA
Input High Voltage	V_{IH}	*	5	2.4	–	2.4	–	–	2.4	–	V
Input Low Voltage	V_{IL}	*	5	–	0.8	–	–	0.8	–	0.8	V
Output Disable Current	I_{DH} I_{DL}	V_{OH}=6.5V V_{OL}=0V *	6.5	–	±0.5	–	$\pm10^{-4}$	±0.5	–	±5	μA
Input Current	I_{IH} I_{IL}	V_{IH}=6.5V V_{IL}=0V *	6.5	–	±0.3	–	$\pm10^{-5}$	±0.3	–	±1	μA
Analog Switch Input Leak Current	I_{OFF}	V_{IH}=6.5V V_{IL}=0V	6.5	–	±0.3	–	$\pm10^{-5}$	±0.3	–	±1	μA
Operating Consumption Current	I_{DD} (opr.)	f_{OSC}=1 MHz	5	–	–	–	1.8	3	–	–	mA
Reference Supply Consumption Current	I_{REF}	V_{REF} = 5V AGND = 0V	5	–	–	–	0.3	0.6	–	–	mA

* Applicable to digital input/output. Not applicable to analog input/output and OSC_{IN}/OSC_{OUT}.

SWITCHING CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, Ta = 25°C, C_L = 50pF)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}		-	50	100	ns
Output Fall Time	t_{THL}		-	40	100	
(Low-High) Propagation Delay Time	t_{pLH}	OSC_{OUT}-GCKO	-	200	400	
(High-Low) Propagation Delay Time	t_{pHL}		-	150	400	
(Low-High) Propagation Delay Time	t_{pLH}	RSEL("L"→"H")-DATA OUT	-	180	400	
(High-Low) Propagation Delay Time	t_{pHL}			150	400	
(Low-High) Propagation Delay Time	t_{pLH}	RSEL("H"→"L")-DATA OUT	-	380	700	
(High-Low) Propagation Delay Time	t_{pHL}		-	300	700	
Output Enable Time	t_{ZL} t_{ZH}		-	80	250	
Output Disable Time	t_{LZ} t_{HZ}		-	280	500	
Max. Clock Frequency	$f_{MAZØ}$	OSC Input	1.5	3.0	-	MHz
Min. Clock Frequency	$f_{MINØ}$	OSC Input	-	-	100	kHz
Input Capacity	C_{IN}	Digital Input	-	4	-	pF
Analog Input Capacity	C_{IN}	$A_0 \sim A_5$	-	7	-	pF
3-State Output Capacity	$C_{ØUT}$		-	8	-	pF

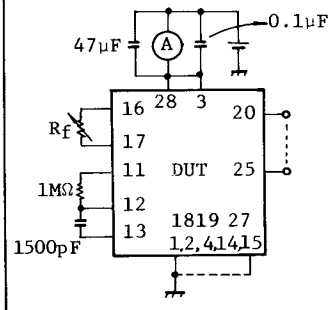
SYSTEM CHARACTERISITCS (Ta = -40 ~ 85°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E_{ZP}	$V_{REF} = V_{DD} = 5V$ $V_{AGND} = 0V$	-	$\pm \frac{1}{4}$	$\pm \frac{1}{2}$	LSB
Full Scale Error	E_{FS}		-	$\pm \frac{1}{4}$	± 1	
Nonlinearity			-	$\pm \frac{1}{4}$	± 1	
STC Min. Pulse Width	t_w		-	-	$\frac{2}{f_{OSC}}$	s
CHS Min. Hold Time	t_{hold}	STC = $CHS_0 \sim 2$	-	-	$\frac{10}{f_{OSC}}+50$	ns
Conversion Time	$t_{conv.}$	$A_{IN} = 0 \sim FS$	$\frac{10^3}{f_{OSC}}$	-	$\frac{3.1 \times 10^3}{f_{OSC}}$	s

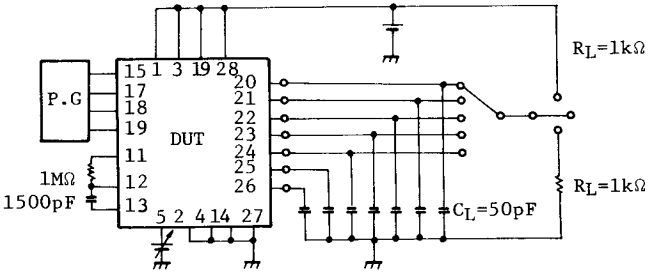
* f_{OSC} : OSC terminal clock frequency [Hz], FS : Full Scale voltage, V_{DD} level

TEST CIRCUIT

IDD(opr.) Test Circuit



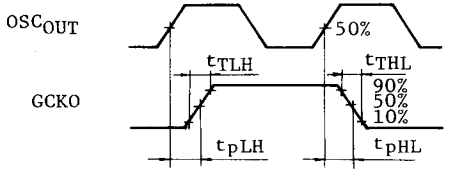
Switching Time Test Circuit



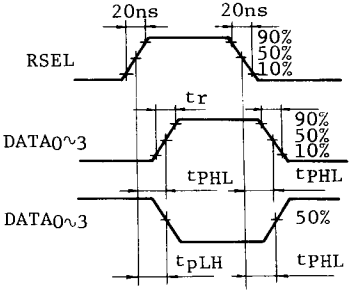
R_f is adjusted as f_{OSC} = 1 MHz.

SWITCHING CHARACTERISTICS TEST WAVEFORMS

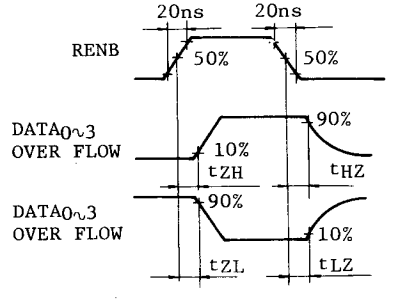
1. tpLH, tpHL (OSC OUT - GCKO)



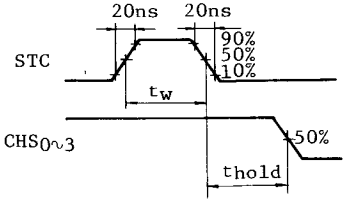
2. tpLH, tpHL (RSEL - DATA)



3. tZL, tZH, tLZ, tZL



4. tw (STC), thold (CHS)



STANDARD CHARACTERISTICS CHARTS

Fig. 1 V_{DD} - $I_{DD(opr)}$

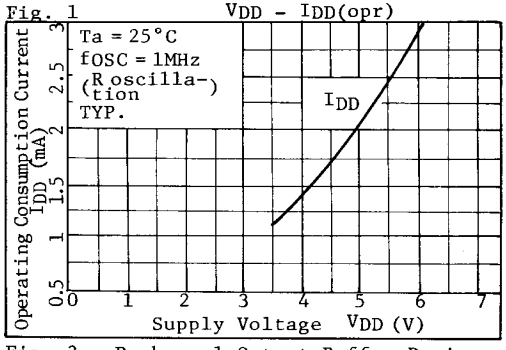


Fig. 2 $I_{DD(opr)}$ - f_{OSC}

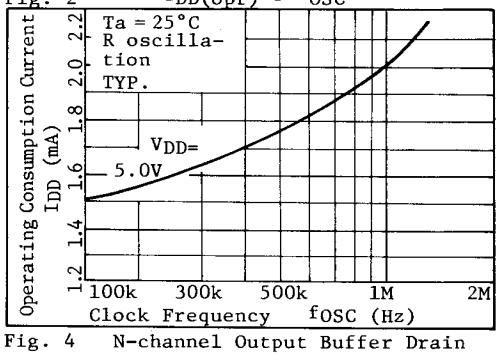


Fig. 3 P-channel Output Buffer Drain Current Characteristics

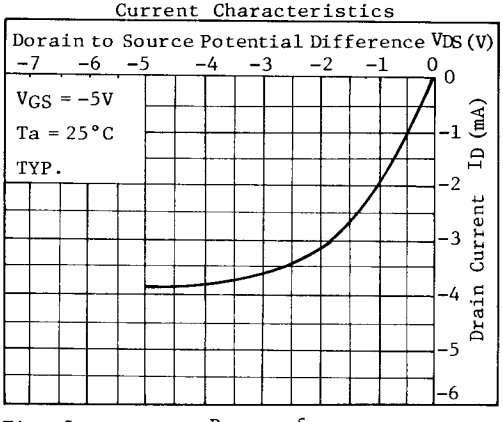


Fig. 4 N-channel Output Buffer Drain Current Characteristics

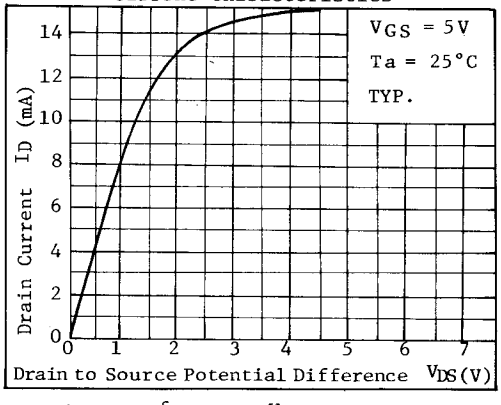


Fig. 5 R_f - f_{OSC}

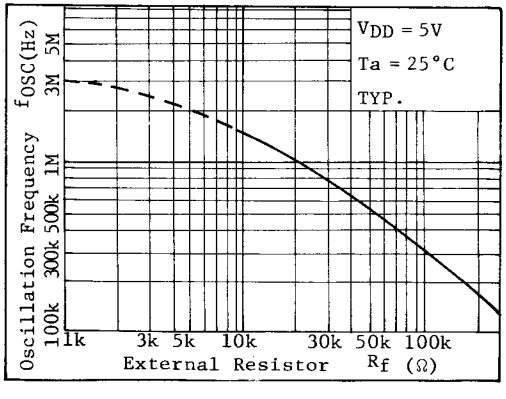


Fig. 6 f_{OSC} - V_{DD}

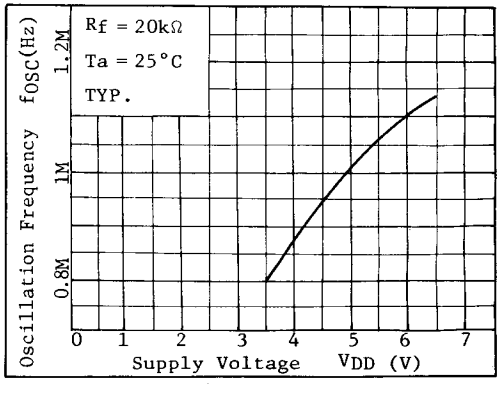


Fig. 7 t_{pd} - V_{DD} (RENB-DATA)

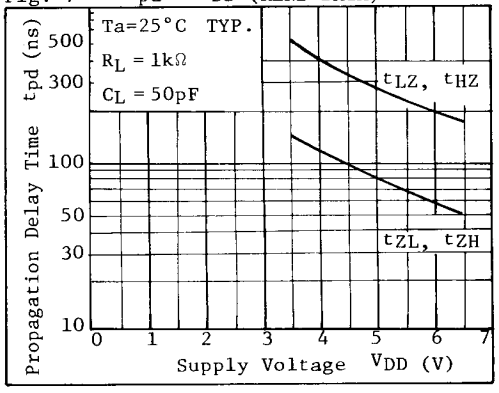


Fig.8 t_{pd} - V_{DD} (RSEL (L→H)-DATA)

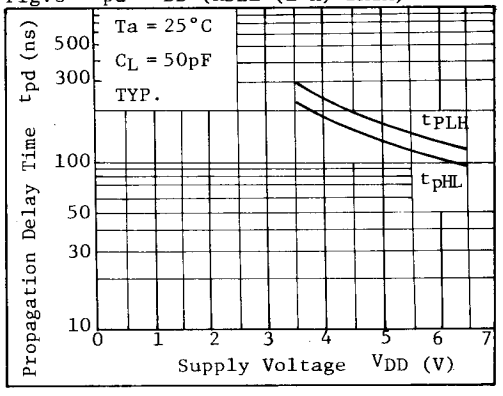


Fig. 9 t_{pd} - V_{DD} (RSEL (H→L)-DATA)

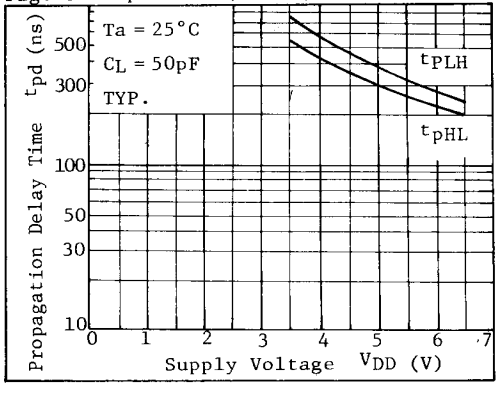


Fig.10 t_{pd} - V_{DD} (OSCOUT - GCKO)

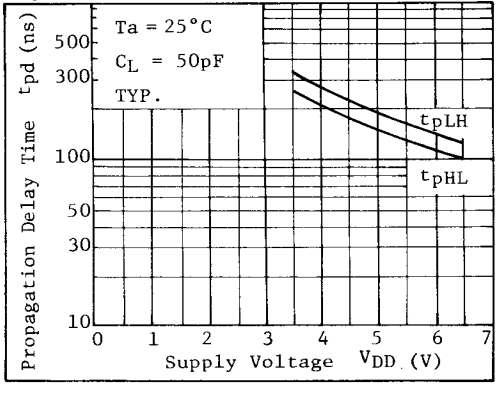
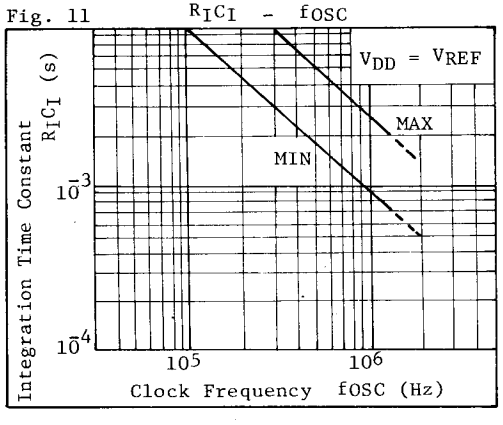


Fig. 11 R_IC_I - f_{OSC}



(Note)
The characterisitcs at left have been prepared for reference at the time of determination of an integrator time constant according to the equation of

$$(R_IC_I = (0.9 \sim 2.5) \cdot \frac{V_{REF}}{V_{DD}} \cdot \frac{10^3}{f_{OSC}} (s))$$

for determing $R_I \cdot C_I$.

In case of the determination of R_I and C_I, the product, or the value, of R_I and C_I is required to be within the range of MIN. to MAX. as shown in left figure after due consideration of dispersion.